S30MS-R ORNAND™ Flash Family

S30MS04GR, S30MS02GR, S30MS01GR, S30MS512R

4 Gb/2 Gb/1 Gb/512 Mb, x8/x16, 1.8 Volt NAND Interface Memory Based on MirrorBit® Technology

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S30MS-R_00 **Revision** 04 **Issue Date** November 2, 2007

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S30MS-R ORNAND™ Flash Family

S30MS04GR, S30MS02GR, S30MS01GR, S30MS512R

4 Gb/2 Gb/1 Gb/512 Mb, x8/x16, 1.8 Volt NAND Interface Memory Based on MirrorBit® Technology

Data Sheet *(Advance Information)*

Distinctive Characteristics

- **Manufactured on 65 nm MirrorBit® Process Technology**
- **Single Power Supply Operation**
  - 1.8 volt read, erase, and program operations
  - V_{CC} = 1.7 V – 1.95 V
- **Bus widths - x8 and x16**
- **Page Size**
  - Full Page: 2K + 64 Byte
  - Partial Page: 512 + 16 Byte
- **Block (erase unit) Architecture**
  - Block Size: 128K + 4K Byte
  - Number of Blocks:
    4 Gb: 4K blocks 2 Gb: 2K blocks
    1 Gb: 1K blocks 512 Mb: 512 blocks
- **Compatible with NAND Flash**
  - Signal and command set compatible with large page/block NAND flash
  - CE# Don't Care
- **Pipelined Read and Write**
  - A second page buffer is used to improve reading and programming throughput
- **One Time Protect (OTP) Area**
  - Eight 2112 byte OTP pages that can be locked individually
- **Erase Suspend and Resume**
  - While Erase is suspended, a read or program operation may be performed
  - An Erase command with any address resumes the last Erase operation
- **3 quality grades for different applications**
  - 100% valid blocks
  - Up to 2% initial bad blocks, no dynamic bad blocks
  - Up to 2% bad blocks including initial and dynamic bad blocks
- **Program/Erase Cycles**
  - 100,000 Program/Erase Cycles per Block Typical
  - 10,000 Program/Erase Cycles per Block Minimum
- **10-Year Data Retention Typical**
- **Operating Temperature Range**
  - Wireless (–25°C to +85°C)
- **Package Options**
  - TSOP: 48-pin
  - FBGA: Multiple MCP Packages Available
  - PoP: Please contact a Spansion sales office for information about our Package on Package offerings.

Performance Characteristics

Read Access Times	
Full Page Random Access	28 µs
Partial Page Random Access	10 µs
Serial Read	25ns

Current Consumption (typical values)	
Read Current	40 mA
Erase Current	60 mA
Program Current	60 mA
Standby Current	10 uA

Typical Program & Erase Times		
	x8	**x16**
Program	2.4 MB/s	2.5 MB/s
Erase	2.6 MB/s	2.6 MB/s
Full Page Read	26.3 MB/s	39.7 MB/s
Pipeline Page Read	38.4 MB/s	75.9 MB/s
Partial Page Read	22.0 MB/s	31 MB/s

Legend:
b = bit, B = Byte

Publication Number S30MS-R_00 **Revision** 04 **Issue Date** November 2, 2007

General Description

The S30MS-R family is made up of single-voltage flash memory products manufactured using 65 nm MirrorBit® technology. The S30MS04GR is comprised of two 2 Gb devices and is organized as 256 M Words or 512 MB. The S30MS02GR is a 2 Gb device organized as 128 Mwords or 256MB. The S30MS01GR is a 1 Gb device, organized as 64 Mwords or 128 MB. The S30MS512R is a 512 Mb device, organized as 32 Mwords or 64 MB.

The S30MS-R family of devices offer advantages such as:

- Fast read speed and reliability suitable for demanding code storage applications
- Fast write and sustained write speed suitable for data storage applications

The devices are offered in a 48-pin TSOP and several FBGA MCP packages.

The S30MS-R family is made up of byte/word serial-type memory devices that use the I/O pins for both address and data input/output, as well as for command input. The Erase and Program operations are automatically executed making the device suitable for applications such as solid-state disks, picture storage for still cameras, cellular phones, and other systems that require high-density non-volatile data storage.

Typical application requirements are shown in the table below.

Application	Minimum Requirements	Spansion ORNAND
2G Network	14.4 Kbps (1.8 KB/sec)	✓
3G r99 Network	2 Mbps (250 KB/sec)	✓
3.5G Network (HSDPA)	14.4Mbps (1.8MB/sec)	✓
2.5G (GRPS)	51 KB/sec up to 108 KB/sec	✓
2.75 (EDGE)	up to 28 KB/sec	✓
USB	1.5 MB/sec	✓
MP3 Playback	320 Kbps (40 KB/sec)	✓
MPEG4 (H.264)	1 MB/sec	✓

The devices include the following features:

- Automatic boot read, allows access of the data in one page after power up, without command and address input of read command.
- Initiation of program and erase functions through command sequences.
- Chip Enable *Don't Care* support for direct connection with microcontrollers.
- The command set is compatible with the large page/block NAND Flash command set.
- Ready/Busy# pin allows the system to monitor the program/erase operation status.
- One Time Protect (OTP) Pages that store permanent information such as a serial number IMEI/ESN information, secure boot code, or SIM-Lock.
- Manufactured using MirrorBit flash technology resulting in the highest levels of quality, reliability, and cost effectiveness.

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1. Definitions

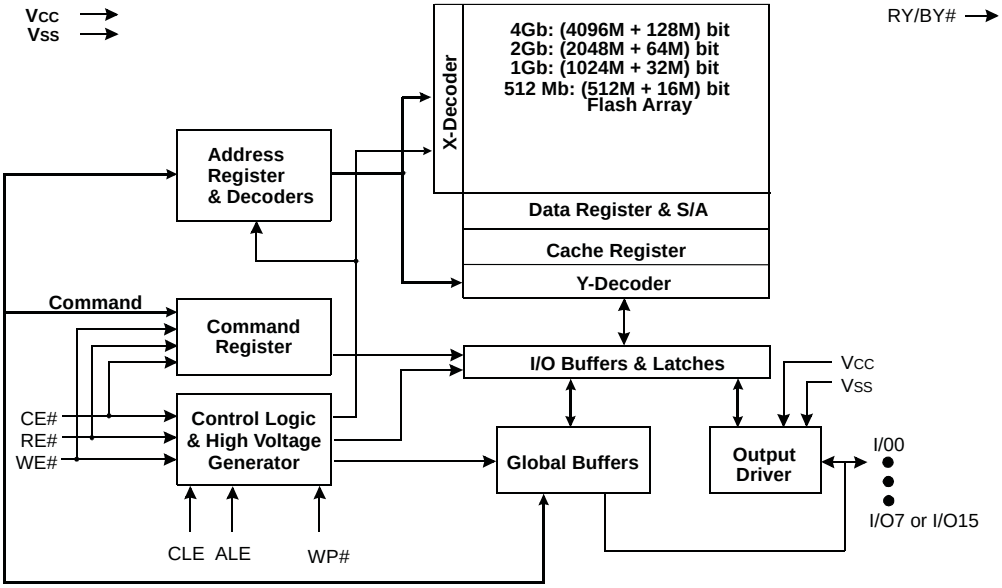
Term	Definition
B	Byte, 8 bits
W	Word, 16 bits
b	Bit
ECC	Error Correction Code
Memory	Flash array
Block	Portion of the memory array that is erased by a single erase operation. Generally 128 KB main area and 4 KB spare area.
Page	Portion of the memory array that may be made available via direct read and write operations of a RAM buffer. Typically a 2-KByte portion of the main area and a 64 Byte portion of the spare area.
Segment	The smallest portion of the memory array that may be read or written. A 512 Byte portion of the main area or a 16 Byte portion of the spare area.

2. Signal Descriptions

The device is a byte/word serial access memory that utilizes time-shared input of commands, address, and data information. The device signals are shown in *Connection Diagrams* on page 16.

Signal	Description
CLE	**Command Latch Enable:** The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O signals on the rising edge of the WE# signal while CE# is low and CLE is High.
ALE	**Address Latch Enable**: The ALE signal is used to control loading of either address information or input data into the internal address/data register. Address information is latched on the rising edge of WE# if CE# is low and ALE is High. Input data is latched if CE# is low and ALE is Low.
CE#	**Chip Enable**: The CE# signal selects the device for data read and command write access. The device enters a low-power Standby mode when CE# is High and no Read, Program, or Erase operation is in progress.
WE#	**Write Enable**: The WE# signal is used to control the acquisition of data from the I/O port. Command, address, and data information on the I/O signals are latched on the rising edge of the WE pulse.
RE#	**Read Enable**: The RE# signal controls serial data output. Data is available t_{REA} after the falling edge of RE#. The internal column address counter is also incremented (Address = Address + 1) on this falling edge.
I/O0 to I/O7	**I/O Port**: The I/O0 to I/O7 signals are used as a port for transferring address, command, and input data to and output data from the device.
I/O8 to I/O15	**I/O Port**: The I/O8 to I/O15 signals are used as a port for transferring input data to and output data from the device in x16 mode only. I/O8 to I/O15 pins must be low level during address and command input.
WP#	**Write Protect**: The WP# signal is used to protect the device from accidental programming or erasing. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.
RY/BY#	**Ready/Busy**: The RY/BY# output signal is used to indicate the operating condition of the device. The RY/BY# signal is in the Busy state (RY/BY# = L) during the Program, Erase, and Read operations and returns to Ready state (RY/BY# = H) after completion of the operation. The output buffer for this signal is an open drain type, allowing the RY/BY# signals of multiple memories to be connected such that a single RY/BY# is provided to the system.
V_{CC}	**Power:** V_{CC} is the power supply.
V_{SS}	**Ground**: V_{SS} is the Ground.
NC	**No Connection**: Lead is not internally connected.
DNU	**Do Not Use**: Signal may be used for manufacturing purposes and must not be connected in system to any signal level.

3. Block Diagram



4. Device Bus Operation

Address input, command input, and data input/output are controlled by the CLE, ALE, CE#, WE#, RE# and WP# signals, as shown in Table 4.1. The operation modes such as Program, Erase, Read, and Reset are controlled by the command operations shown in Table 4.1.

Table 4.1 Operation Table

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input
L	L	L	H	↓	X	Sequential Read or Status Output	
H	L	L	↑	H	H	Program or Erase	Command Input
L	H	L	↑	H	H		Address Input
L	L	L	↑	H	X	Data Input	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0 V or V_{CC} (1)	Stand-by	

Legend

H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}

Notes

1. *WP# should be biased to GND or V_{CC} for lowest standby power.*
2. *In Stand-by mode the device power consumption is lowered to the Stand-by power level only when internal Read, Program, or Erase operations are completed. Until all operations are complete the device still draws active level power.*

4.1 CE# Don't Care Feature

CE# does not need to be continuously asserted across command and address write operations or during busy periods as was required by some earlier generation NAND interface devices.

4.2 Stacked Die Product

A 4 Gb device is built from two stacked 2 Gb devices. The pinout of the stacked product has a single CE# pin and can be addressed as a single die solution.

In the stacked die product, the most recently activated die accepts the command. The following commands do not require an address in order to execute. Before issuing these commands, the system should issue an address-carrying-command in order to select the correct die.

- ID Read
- Read Column Address Change
- Reset or Erase Suspend
- Status Read
- OTP Commands

When the reset/erase suspend command is issued by the system, the most recently activated die receives the command. In the case where the device is erasing, the device suspends erase. In the case where the device is not erasing the die resets. Note that only one die will be reset. To reset both die in a stacked die product, the reset command should be entered to reset the most recently accessed die. Then an address carrying command should be entered to the non-active die. Once the second die has been activated another reset command can be entered to reset the second die.

In addition, when one of two dies is performing some embedded operation, the input command of Program, Erase and Read is prohibited.

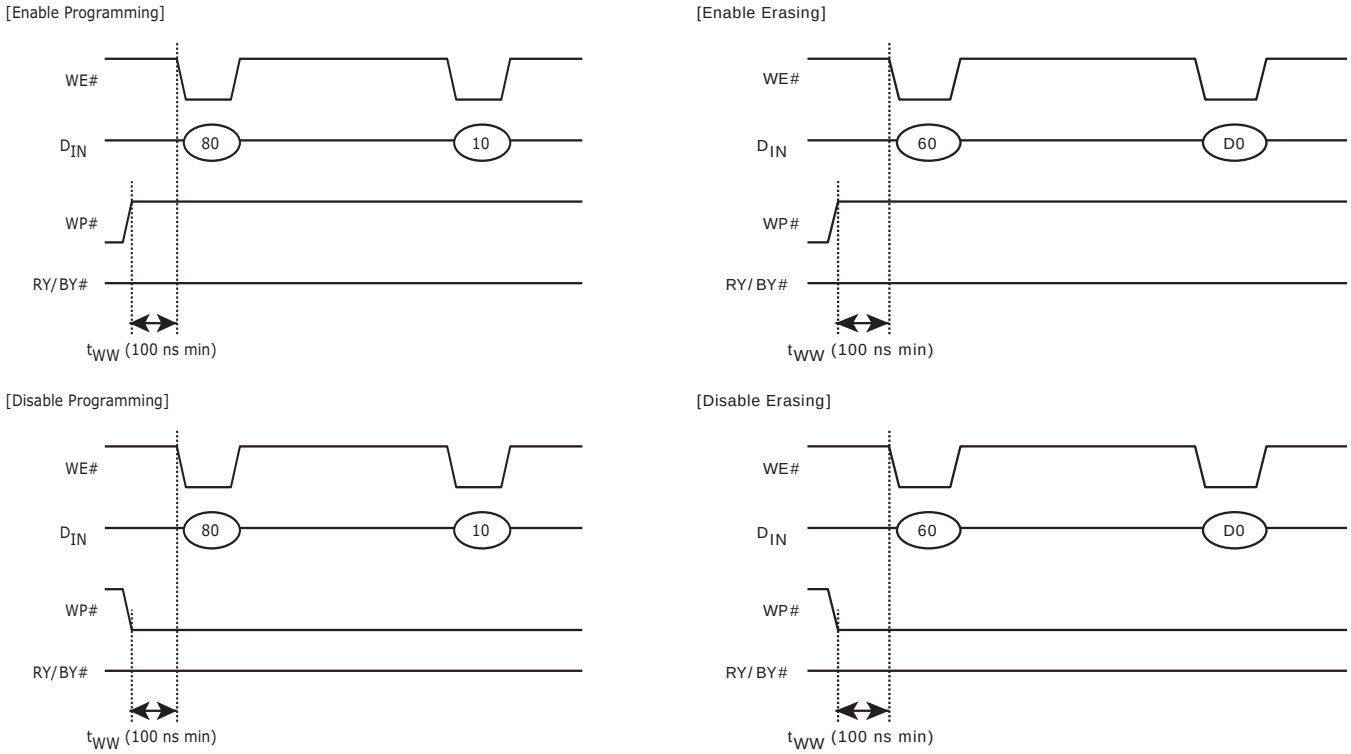
Amax + 1	CE#	Comments
0	0	Device 0 Selected; Device 1 Standby
1	0	Device 1 Selected; Device 0 Standby

Note
Amax +1 = A29 for x8 devices and A28 for x16 devices.

4.3 WP# Signal Timing

The state of the WP# signal is checked only at the beginning of a program or erase operation. If WP# is low an operation cannot start. The user should keep the WP# pin either high or low during the complete command and program/erase operation. The level of the WP# pin may be changed after the erase and/or program is complete. The operations are enabled and disabled as shown in the following timing diagrams:

Figure 4.1 WP# Signal—Low

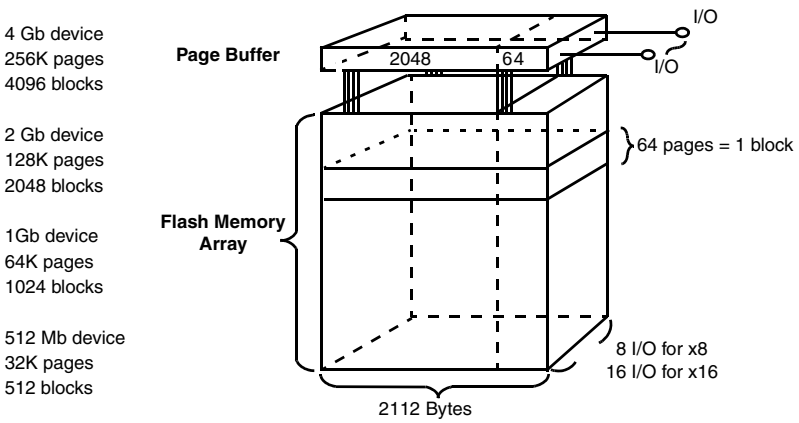


5. Internal Memory Array Organization

The Program operation works on page units while the Erase operation works on block units.

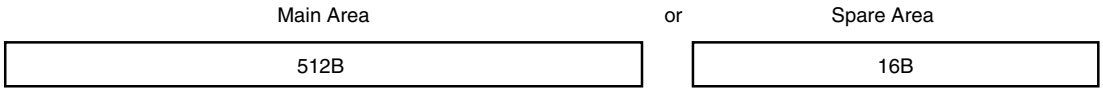
5.1 Array Organization

Figure 5.1 Array Organization

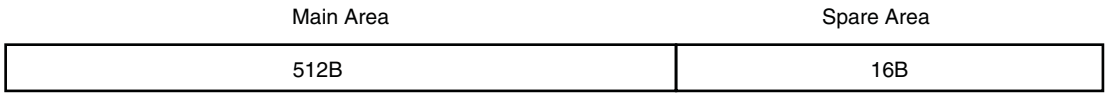


The memory array is divided into a main memory area and a related spare area. A page consists of 2112 Bytes in which 2048 Bytes are used for main memory storage and 64 Bytes are used as a spare area for redundancy or other uses. Each page is divided into eight segments, four 512-Byte main-area segments and four 16-Byte spare-area segments.

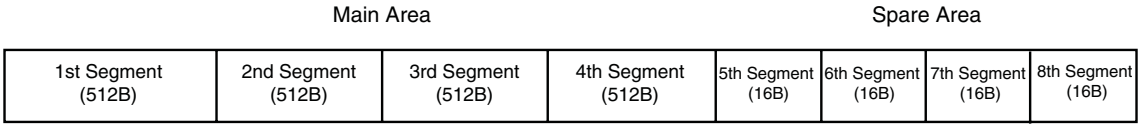
Segment



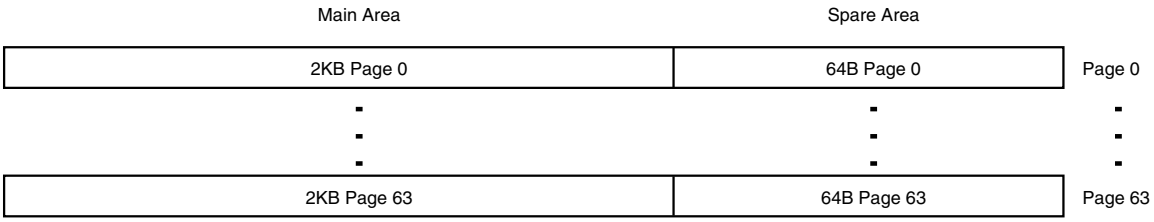
Partial Page



Page



Block



Array

Density	# Blocks	Block Size	Pages per Block
4 Gb	4096	128 KB	64
2 Gb	2048	128 KB	64
1 Gb	1024	128 KB	64
512 Mb	512	128 KB	64

Table 5.1 shows a summary of the addressing for the memory array components.

Table 5.1 Memory Addressing Key

Density	Bus Width	Row Address		Column Address					Blocks
		Block Address	Page Address in Block	Main/Spare Area	Main Page Segment	Main Column Address	Spare Page Segment	Spare Column Address	
4 Gb	x8	A29:A18	A17:A12	A11 (0=Main, 1=Spare)	A10:A9	A8:A0	A5:A4	A3:A0	2 x 2048 (See Note)
4 Gb	x16	A28:A17	A16:A11	A10 (0=Main, 1=Spare)	A9:A8	A7:A0	A4:A3	A2:A0	2 x 2048 (See Note)
2 Gb	x8	A28:A18	A17:A12	A11 (0=Main, 1=Spare)	A10:A9	A8:A0	A5:A4	A3:A0	2048
2 Gb	x16	A27:A17	A16:A11	A10 (0=Main, 1=Spare)	A9:A8	A7:A0	A4:A3	A2:A0	2048
1 Gb	x8	A27:A18	A17:A12	A11 (0=Main, 1=Spare)	A10:A9	A8:A0	A5:A4	A3:A0	1024
1 Gb	x16	A26:A17	A16:A11	A10 (0=Main, 1=Spare)	A9:A8	A7:A0	A4:A3	A2:A0	1024
512 Mb	x8	A26:A18	A17:A12	A11 (0=Main, 1=Spare)	A10:A9	A8:A0	A5:A4	A3:A0	512
512 Mb	x16	A25:A17	A16:A11	A10 (0=Main, 1=Spare)	A9:A8	A7:A0	A4:A3	A2:A0	512

Note
The 4 Gb device is a two-die stack of the 2 Gb device with each device having the same memory architecture as the 2 Gb.

An address is loaded through the I/O port over four or five consecutive address write cycles, as shown in Tables 5.2 – 5.4. If a fifth address cycle is written to a device that needs only 4 cycles, the fifth address cycle is ignored. If a fifth address cycle is not written to a device that needs one the fifth address is treated as having a zero value. The ***Notes*** for Tables 5.2 – 5.4 and are listed below Table 5.4.

Table 5.2 (2 Gb and 4 Gb) x 8 device

2 Gb and 4 Gb	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27
5th Cycle	A28	A29 (Note 4)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)

Table 5.3 (1 Gb) x 8 device

1 Gb	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27

Table 5.4 (512 Mb) x8 Addressing

512 Mb	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	L (Note 1)

Notes

1. *L = V_{IL}.*
2. *A0 to A11:Column address (12 bits for 2,112 Bytes).*
   A12 to A28: Row address, consists of:
   A12 to A17: Page address in block (6 bits for 64 pages).
3. *A18 to A28: Block address (4 Gb and 2 Gb device: A18 to A28, 11 bits for 2048 blocks; 1 Gb device: A18 to A27, 10 bits for 1024 blocks; 512 Mb device: A18 to A26, 9 bits for 512 blocks.)*
4. *4 Gb device is same die stack of 2 x 2 Gb devices. Therefore, 4 Gb devices have the same addressing as 2 Gb devices. 4 Gb has one single CE#, A29 is used to select any 2 Gb stacked devices to create 4 Gb device.*

The ***Notes*** for Tables 5.5 – 5.7 and are listed below Table 5.7.

Table 5.5 (2 Gb and 4 Gb) x 16 Addressing

2 Gb and 4 Gb	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	I/O8 – I/O15
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	L (Note 1)
2nd Cycle	A8	A9	A10	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18	L (Note 1)
4th Cycle	A19	A20	A21	A22	A23	A24	A25	A26	L (Note 1)
5th Cycle	A27	A28 (Note 4)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)

Table 5.6 (1 Gb) x 16 Addressing

1 Gb	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	I/O8 – I/O15
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	L (Note 1)
2nd Cycle	A8	A9	A10	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18	L (Note 1)
4th Cycle	A19	A20	A21	A22	A23	A24	A25	A26	L (Note 1)

Table 5.7 (512 Mb) x 16 Addressing

512 Mb	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	I/O8 – I/O15
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	L (Note 1)
2nd Cycle	A8	A9	A10	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18	L (Note 1)
4th Cycle	A19	A20	A21	A22	A23	A24	A25	L (Note 1)	L (Note 1)

Notes

1. *L = V_{IL}.*
2. *A0 to A10:Column address (11 bits for 1,056 words)*
3. *A11 to A27: Row address, consists of:*
   A11 to A16: Page address in block (6 bits for 64 pages). A17 to A27: Block address (4 Gb and 2 Gb device: A17 to A27: 11 bits for 2048 blocks; 1 Gb device: A17 to A26: 10 bits for 1024 blocks; 512 Mb device: A17 to A25: 9 bits for 512 blocks.)
4. *4 Gb device is same die stack of 2 x 2 Gb devices. Therefore, 4 Gb devices have the same addressing as 2 Gb devices. 4 Gb has one single CE#, A28 is used to select any 2 Gb stacked devices to create 4 Gb device.*

6. Ordering Information

The ordering part number is formed by a valid combination of the following:

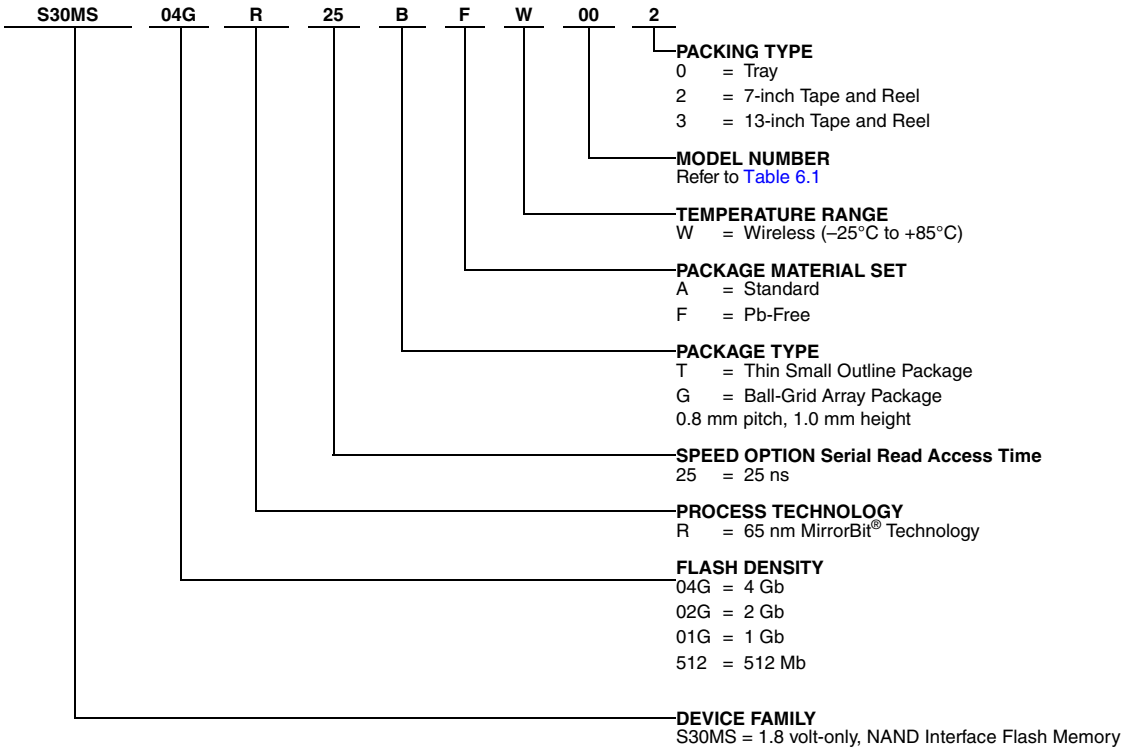


Table 6.1 Model Numbers

Bus Width	2-bit Detect-1bit Fix ECC Required	Bad Blocks	Model Number
x8	No	None	00
x8	No	Up to 2% initial No bad blocks during life	10
x8	Yes	Maximum 2% over lifetime	20
x16	No	None	01
x16	No	Up to 2% initial No bad blocks during life	11
x16	Yes	Maximum 2% over lifetime	21

Note
The first block is guaranteed to be a valid block

6.1 Valid Combinations

Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations				
Base Ordering Part Number	**Speed Option**	**Package Type, Material, and Temperature Range**	**Model Number**	**Packing Type**
S30MS04GR	25	TFW	00, 01, 10,11,20,21	0, 3 (Note 1)
S30MS02GR				
S30MS01GR S30MS512R				

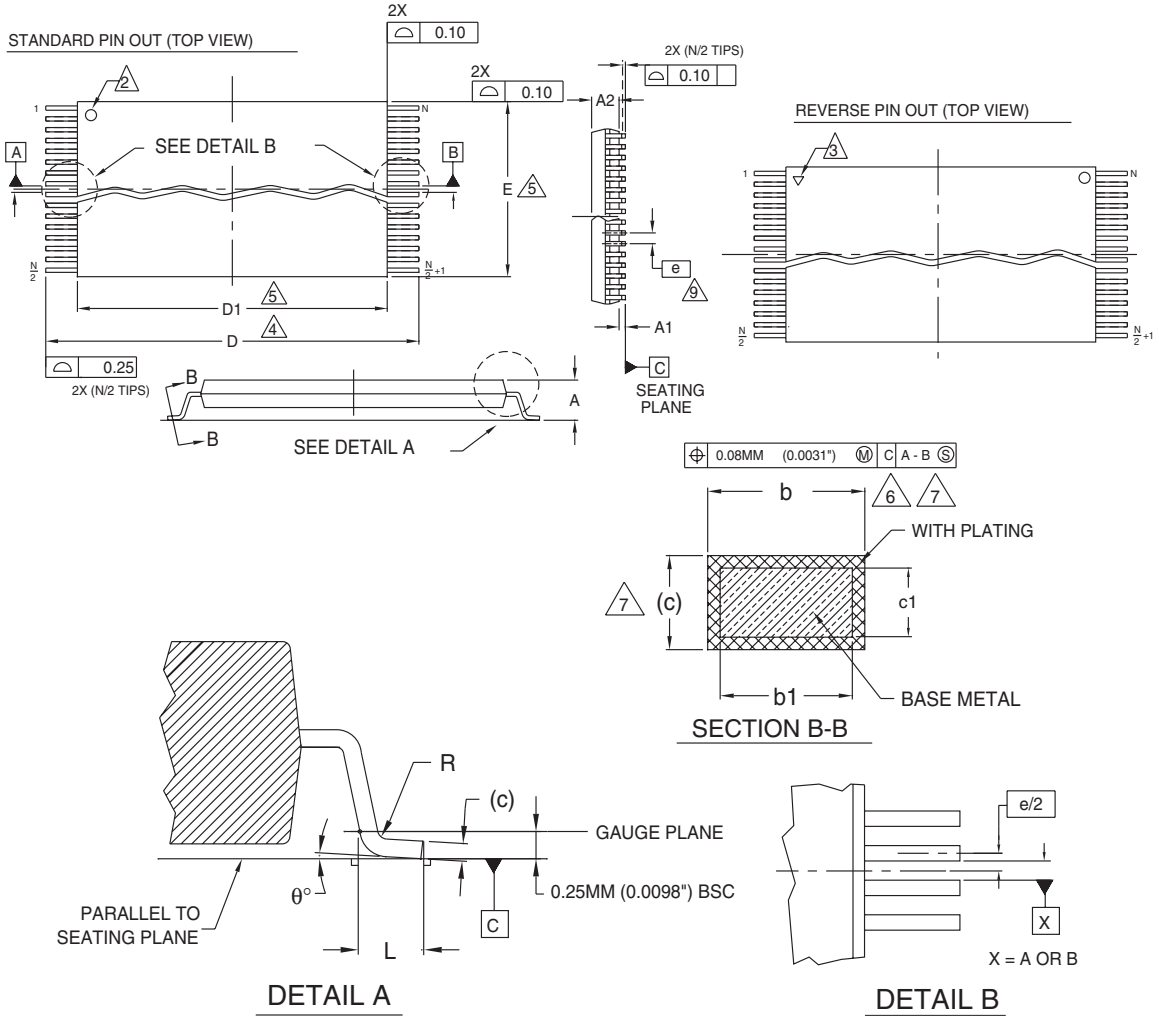
Note
1. *Type 0 is standard. Specify other options as required.*

7. Connection Diagrams

7.1 TSOP 48-Pin Pinout

8. Physical Dimensions

8.1 48-Pin TSOP



Package	TS/TSR 048		
Jedec	MO-142 (D) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8°
R	0.08	—	0.20
N	48		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN), INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08 (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10MM (.0039") AND 0.25MM (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

3355 \ 16-038.10c

9. Device Operation

9.1 Commands

Table 9.1 Command Table

Function	1st Cycle	2nd Cycle	Command Accepted During Busy State
Page Read	00h	30h	No
Partial Page Read	00h	31h	No
Pipeline Read - Full Page	00h	32h	No
Pipeline Read - Full Page No Additional Requests	00h	33h	No
Read for Page Duplicate	00h	35h	No
ID Read	90h	—	No
Page Program	80h	10h	No
Cache Program	80h	15h	No
Page Duplicate Program	85h	10h	No
Data Input for Column Address Change	85h	—	No
Read Column Address Change	05h	E0h	No
Block Erase/Erase Resume	60h	D0h	No
Reset or Erase Suspend	FFh	—	Yes
Status Read	70h	—	Yes
OTP Area Overlay	B0h	00h	No
OTP Area Remove	B0h	01h	No
OTP Page Protection Status	B0h	02h	No
OTP Area Default as Overlay	B0h	03h	No
OTP Area Default as Removed	B0h	04h	No
OTP Protect Page	B0h	05h	No

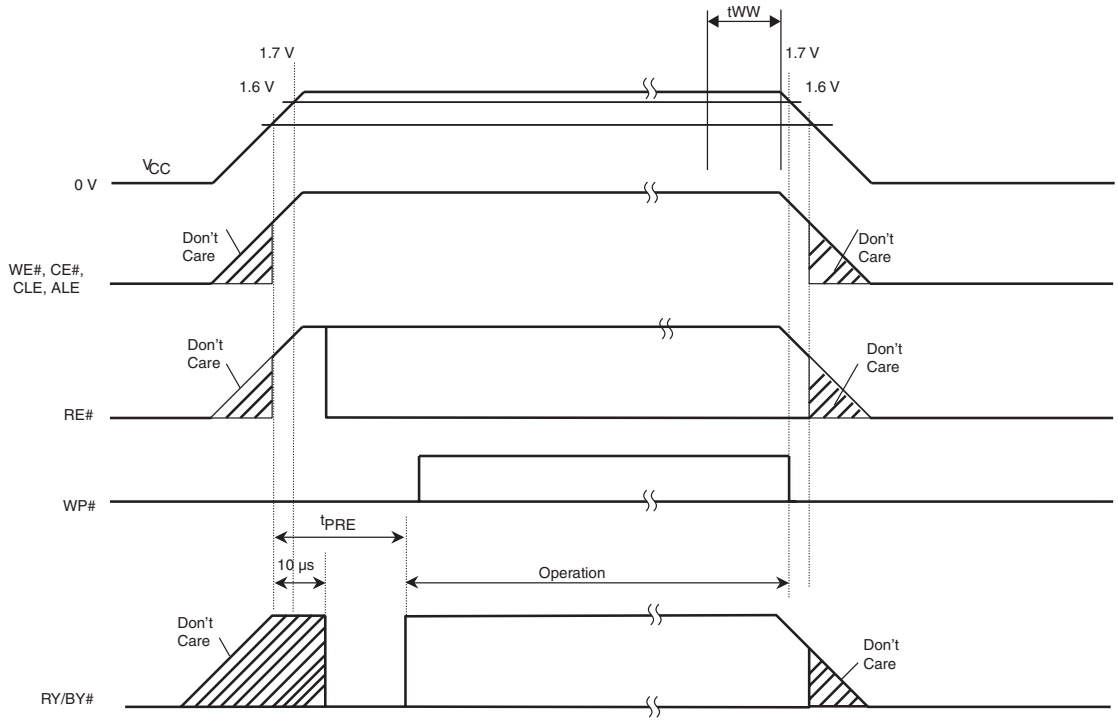
Notes

1. *Random Data Input/Output can be executed in a page or a partial 1/4 page.*
2. *Input of a command (other than those specified above) is prohibited. If an unknown command is entered during the command cycle is undefined. A reset command may be required to return the device to a known idle state.*
3. *During the Busy state, input commands are restricted to 70h and FFh.*
4. *During Erase Suspend, the FFh command is restricted. All other commands are prohibited.*

9.2 Power On and Power Off

During power transitions the control signals are don't care and data is protected while V_{CC} is below 1.6 V. After V_{CC} exceeds 1.6 V the device performs internal initialization operations.

Figure 9.1 Power-On/Off Sequence



During power transitions the control signals do not affect the device state while V_{CC} is below 1.6 V. When V_{CC} reaches 1.6 V, the device is above its lockout voltage and the control pins must follow the timing diagram in Figure 9.7. During this time CE# must remain high because the device cannot receive commands until the state machine is active.The RD/BY# pin will go low and indicate when the state machine is active. It is recommended that the WP# pin remain low during this time to protect the data during voltage stabilization.

At power-off WP# should be utilized to protect the device during the power transition. It is recommended to assert WP# low t_{WW} before V_{CC} begins the ramp down.

9.2.1 Power-On Read

During the power-on sequence the device will automatically load data into the output buffers. This feature enables the system to read boot code without issuing any commands, which is generally used for shadowing architectures that require automatic boot code download into buffer RAM.

To use this feature the system must wait t_{PRE} after V_{CC} has sustained 1.6 V during the power ramp. The system can also determine that the data is loaded by monitoring the RD/BY# pin or by monitoring the status register. At power-on the state machine will become active 10 µs after ramp causing the RD/BY# pin to go low and the device status to show active. When the data is loaded into the register the device go to a standby state.

The default state for the device is to load page 0 into the output buffers, but it is also possible to configure the device so that it will load OTP data into the buffers at power-on. Refer to Section 9.10 for more information on using default OTP overlay to read OTP data in the power-on sequence.

9.3 ID Read

The ID Read command may be used to identify the manufacturer, type, density, and other features of the device. The 90h command is issued, followed by a single address cycle of value zero. Then a sequence of words or bytes may be read to identify the device. For devices with word (16-bit) wide data bus the ID information appears in the lower byte of the data bus on I/O0-I/O7, I/O8-I/O15 are undefined. Each toggle of the RE# signal delivers a new word or byte depending on the device data bus width. The meaning of the ID byte sequence is shown in Table 9.2 on page 20 through Table 9.5 on page 21. Data read beyond the fifth byte is undefined.

Figure 9.2 ID Read Operation

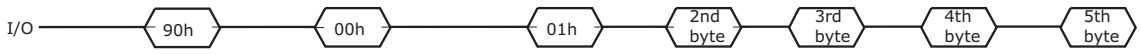


Table 9.2 ID Byte Settings Summary

Byte	Description		Hex Data
1st Byte	Maker Code		01h
2nd Byte	Device Code 1st Byte	512 Mb (x8)	81h
		512 Mb (x16)	91h
		1 Gb (x8)	A1h
		1 Gb (x16)	B1h
		2 Gb (x8)	AAh
		2 Gb (x16)	BAh
		4 Gb (x8)	CCh
		4 Gb (x16)	DCh
3rd Byte	Device Code 2nd Byte	ECC/ECC-Free	11h
4th Byte	Block Size, Simultaneous Programmed Pages, RFU		00h
5th Byte	Page Size, Spare Size, RFU		22h
6th Byte	RAM and Other MCP identifiers		00h

Note
In x16, I/O 15 – I/O 8 = 00h

Table 9.3 4th ID Byte

Description		I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
Block Size: 128 KBytes		X	X	X	X	X	0	0	0
Block Size: 512 KBytes		X	X	X	X	X	0	0	1
Block Size: 2048 KBytes		X	X	X	X	X	0	1	0
Number of simultaneously programmed pages	1	X	X	X	0	0	X	X	X
	2	X	X	X	0	1	X	X	X
	4	X	X	X	1	0	X	X	X
	8	X	X	X	1	1	X	X	X

Table 9.4 5th ID Byte

Description	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
Page Size: 512 Bytes	X	X	X	X	X	0	0	0
Page Size: 1024 Bytes	X	X	X	X	X	0	0	1
Page Size: 2048 Bytes	X	X	X	X	X	0	1	0
Page Size: 4096 Bytes	X	X	X	X	X	0	1	1
Page Size: 8192 Bytes	X	X	X	X	X	1	0	0
Spare Size: 0 Bytes	X	X	0	0	0	X	X	X
Spare Size: 8 Bytes	X	X	0	0	1	X	X	X
Spare Size: 16 Bytes	X	X	0	1	0	X	X	X
Spare Size: 32 Bytes	X	X	0	1	1	X	X	X
Spare Size: 64 Bytes	X	X	1	0	0	X	X	X

Table 9.5 6th ID Byte

Description	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
RAM and Other MCP Identifiers: Reserved for Future Use	X	X	X	X	X	X	X	X

9.3.1 Read Mode

During a read operation the device transfers one page of data from the memory array to a page buffer. After the data is transferred it is available for sequential byte/word access through a sequential read operation as shown in Table 4.1 on page 10.

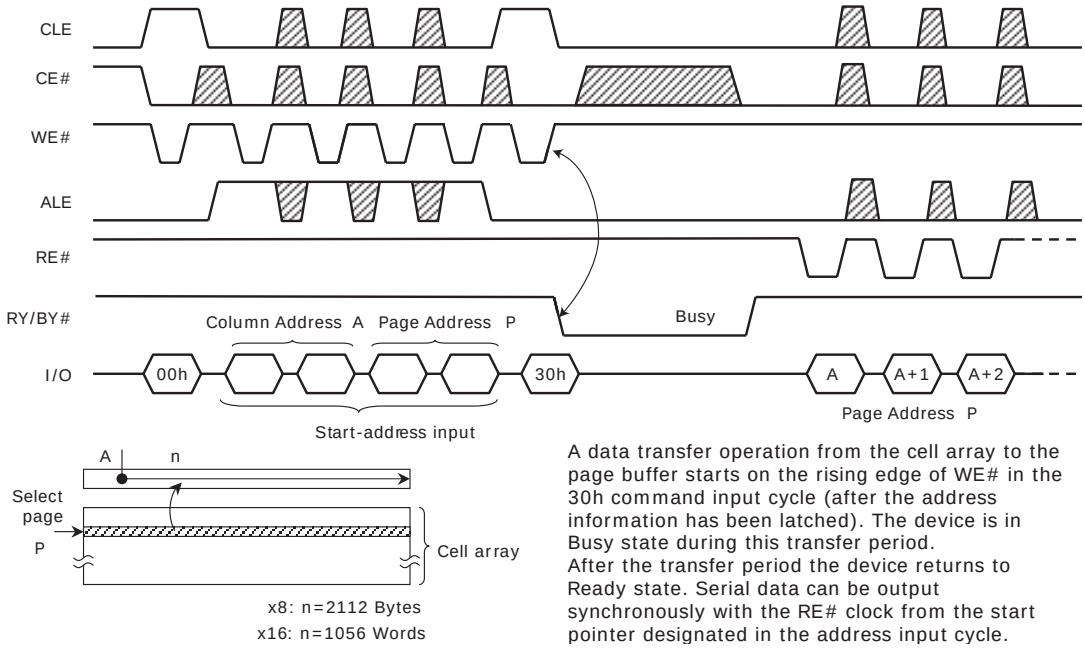
See Figure 9.3 on page 22 for timing details.

The Read Column Address Change command allows the system to read from any location within a page, and may be issued multiple times by four or five address write cycles, depending on the device density, followed by a 31h command.

A partial page read loads one main array area segment and its related spare area (512 + 16 Bytes) into the page buffer as shown in Table 9.6 on page 25. Because less data is loaded from the memory array a partial page read offers faster access time than a full page read.

In a partial page read, if the address of the 1st segment is chosen, the 1st (Main) and 1st (Spare) segments data are loaded to the output buffer together. The 5th segment data is read out following the 1st segment data.

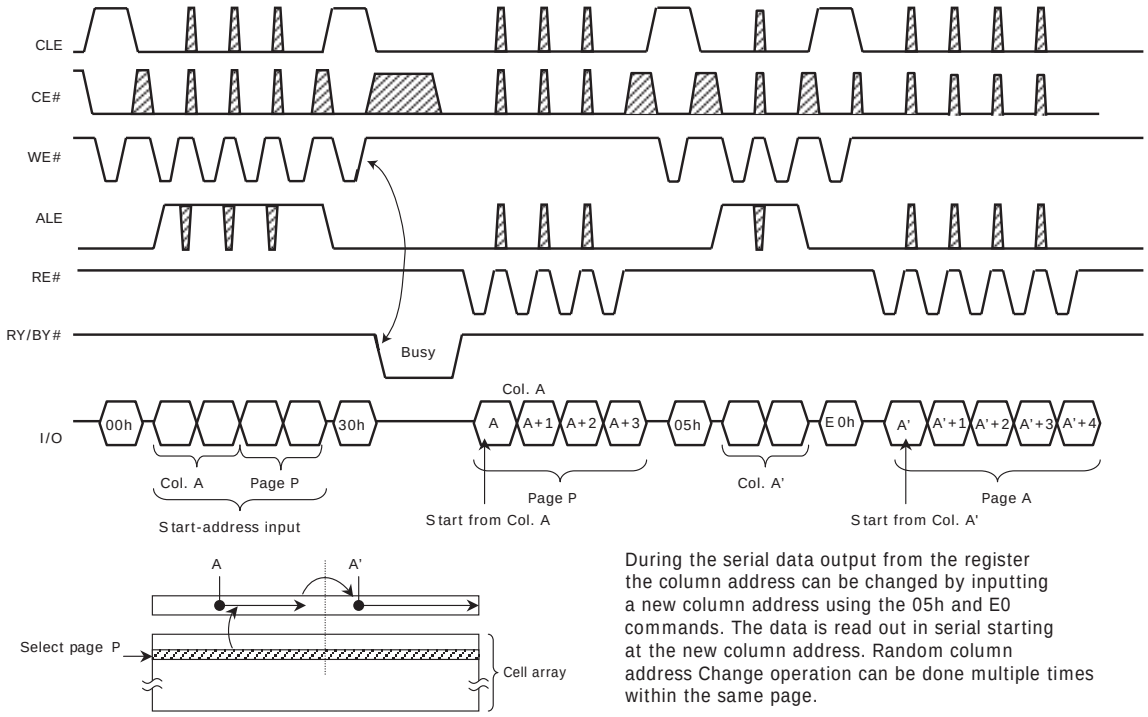
Figure 9.3 Read Mode



Note

1 Gb and 512 Mb devices require four cycles to load the addresses. An additional page address is needed for 2 Gb and 4 Gb devices.

Figure 9.4 Column Address Change Read



Note

1 Gb and 512 Mb devices require four cycles to load the addresses. An additional page address is needed for 2 Gb and 4 Gb devices.

9.4 Pipeline Read

Pipeline read is a feature that caches sequential or random pages to achieve higher sustained read rates.To use pipeline read, the system should initiate a read command for page X. After RY/BY# goes high and prior to reading data from the device, the pipeline read command can be issued for a subsequent page X+1 to load into the cache. Once the Pipeline read command, 32h, has been entered the system can read page X from the output while the secondary buffer is loaded with page X+1. This command sequence can be repeated to sequentially read pages until the command entry for the final page.

The address load command (00h) stops the prior read from page X and transfers the next page X+1 from the cache register to the output buffer. To continue with pipeline read the 32h input should be entered after the address input. If the system is on the final read cycle, a dummy address followed by 33h should be entered to indicate that the final page can be loaded to the buffer without a subsequent address load command.

Pipeline Read is recommended for use with full pages. In the case where less than half of the page is read in a cycle, the system must wait 25us between entry of the Pipeline Read Command (32h) and the subsequent address load command (00h).

Pipeline Read synchronization can be achieved by either monitoring RY/BY# or with the status read command. Please refer to Figure 9.5 when using RY/BY# and Figure 9.6 when using Status Read Command.

Figure 9.5 Pipeline Read Mode

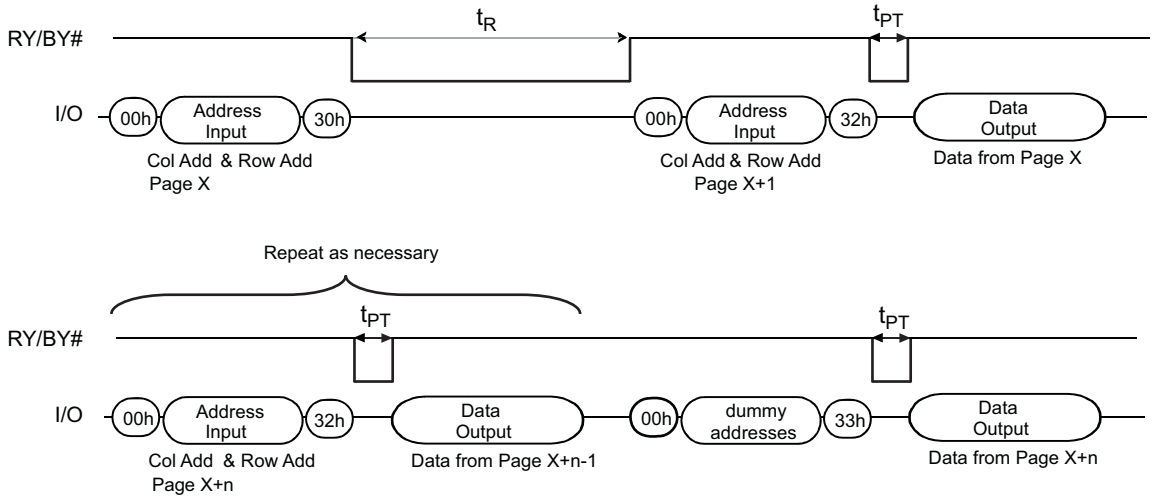
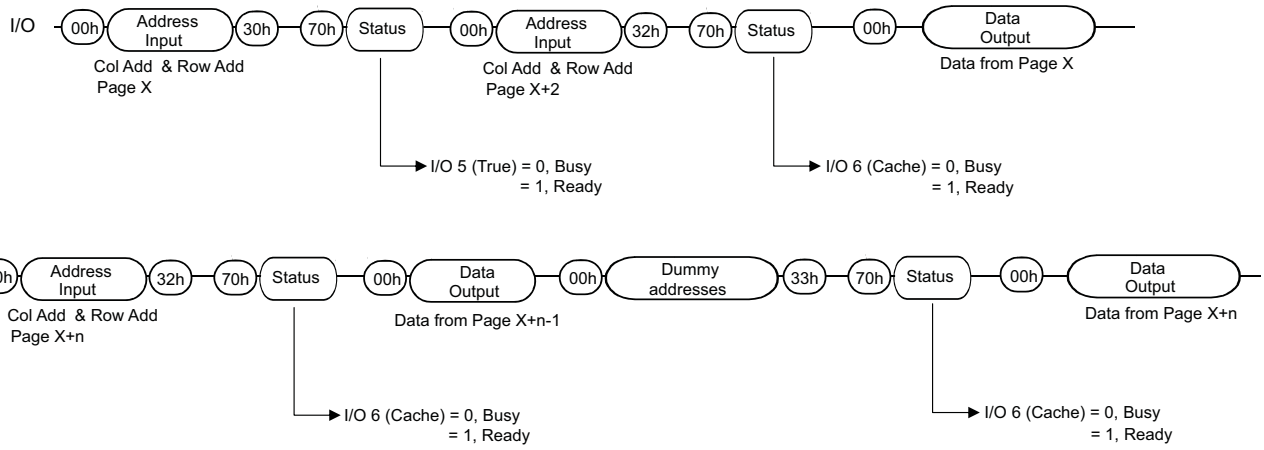


Figure 9.6 Pipeline Read Mode without RY/BY#



9.5 Page Program

The device conducts a Page Program operation when it receives a 10h Program confirm command after the address and data are input. The sequence of command and address and data input is shown below. (See Figure 9.7.)

Partial page programming is allowed for this device. A page is divisible into eight segments and each segment may be programmed individually or in any combination of segments simultaneously. For example, in x8 devices the first data segment of 512 bytes and the first spare area segment of 16 bytes, are programmable at the same time. Table 9.6 describes the page segments:

Table 9.6 Page Segments

	x8	x16
Data Area (Segment)	**512 Bytes x 4 Segments/Page (Column Address)**	
1st	0 to 511	0 to 255
2nd	512 to 1023	256 to 511
3rd	1024 to 1535	512 to 767
4th	1536 to 2047	768 to 1023
Spare Area (Segment)	**16 Bytes x 4 Segments/Page (Column Address)**	
5th	2048 to 2063	1024 to 1031
6th	2064 to 2079	1032 to 1039
7th	2080 to 2095	1040 to 1047
8th	2096 to 2111	1048 to 1055

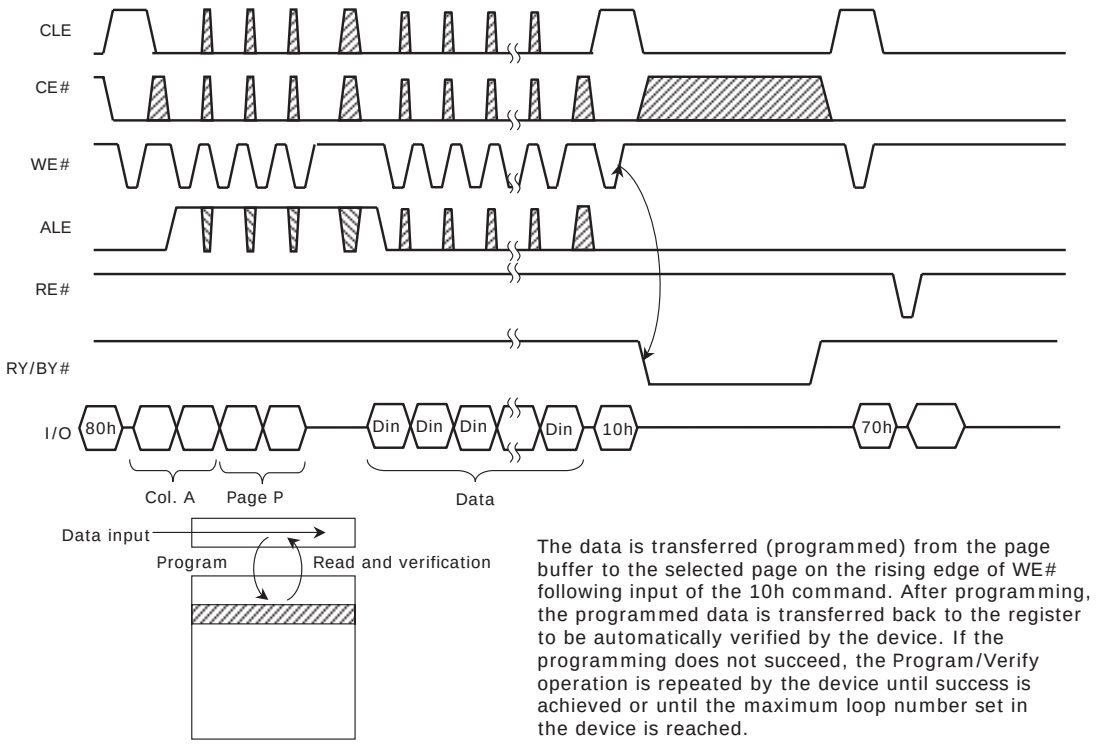
The maximum number of consecutive partial page program operations allowed in the same segment is one. Each of the eight segments may be programmed once before a block erase is required. Once a segment is programmed, any subsequent writes to the same segment without erase causes the initial data in the segment to become invalid. The data written during the second write will be valid.

The device also supports random data programming within a page by using the random data input command (85h). Random data input requires the command to be entered between column addresses during the page program command cycle. Once the new column address is entered, the system can continue the page program command cycle by entering the page address and the data. The Page Program confirm command (10h) initiates the programming operation.

Once the program operation starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the RY/BY# output, or the Status bit (I/O5) of the Status Register. When the Page Program is complete, the Status Bit (I/O0) may be verified. The internal write verify detects only errors for 1s that are not successfully programmed to 0s. The command register remains in Read Status command mode until another valid command is written to the command register.

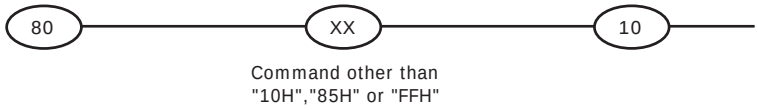
Only the Read Status command and Reset command are valid while programming is in progress. Entering any other command puts the device into an unknown state.

Figure 9.7 Page Program



Once the Serial Input command 80h is input, the only acceptable commands are the programming commands 10h, 85h or the Reset command FFh. If any other input command is used, the program operation is not performed and the device must be reset.

Figure 9.8 Serial Input Command Sequence Error



9.6 Cache Program

Cache Program is a double buffer scheme for faster programming. The Cache buffer size is identical to the page buffer size (2112 B). Data may be written into the cache register while other data previously stored in the page buffer are programmed into the memory array.

After writing the first set of data (up to 2112 B) into the cache register, the Cache program command (15h) must be entered instead of the standard Page Program command (10h) in order to free up the cache register and start the internal program operation. When data is transferred from the cache register to the data register, the device remains in the Busy state for a short period of time (t_{CBSY}) then the cache register is ready for the next data-input. The Read Status command (70h) may be issued to verify that the cache register is ready by polling the Cache-Busy status bit (I/O6). Pass/Fail status of the previous page is available upon the return to the Ready state. When the next set of data is input with the Cache Program command, t_{CBSY} is affected by the progress of pending internal programming. The programming of the cache register is initiated only when the pending program cycle is finished and the data register is available for the transfer of data from the cache register. The status bit (I/O5) for internal Ready/Busy may be polled to identify the completion of internal programming.

If the system monitors the progress of programming with RY/BY# only, the last page of the target programming sequence must be programmed with Page Program command (10h). Alternatively, if the last page to be programmed is accomplished using the Cache Program command (15h), status bit (I/O5) must be polled to verify that the last program is actually finished before starting other operations.

Following the Cache Program Command (15h), the pass/fail status information is available as follows:

1. I/O1 returns the status of the previous page (when ready or when the I/O6 bit is changing to a *1*).
2. I/O0 returns the status of the current page (upon true ready, or when the IO5 bit is changing to a *1*).
3. I/O0 and I/O1 may be read together.

The WP# signal is either low during the entire cache program sequence to lock all the programs or it is high to allow programming. The WP# signal needs to be fixed before the first cache program command is input. Please refer to *WP# Signal Timing* on page 11.

Figure 9.9 Cache Program with RY/BY# Only Monitored

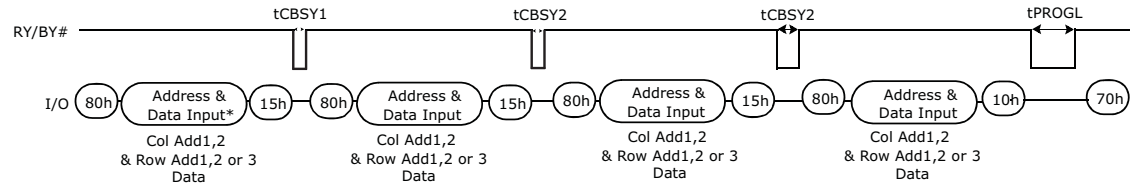
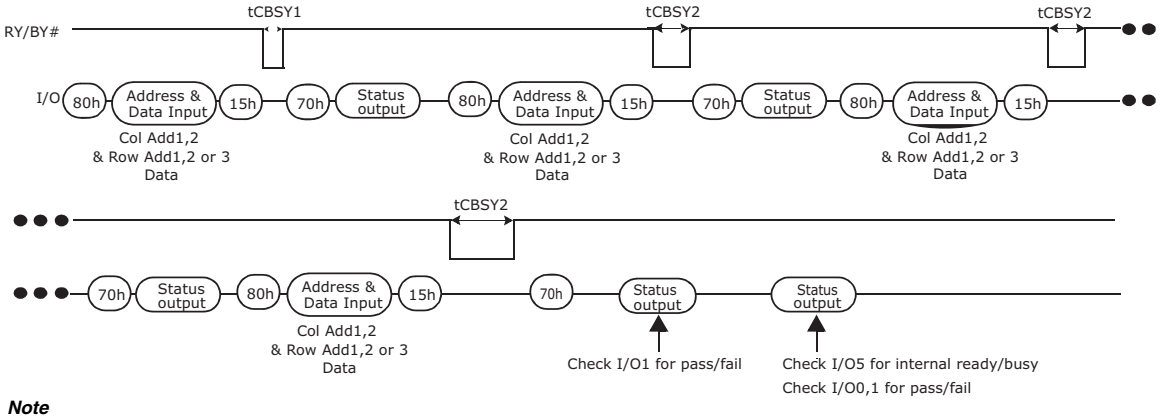


Figure 9.10 Cache Program Monitored by Status Register



Note

Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula: t_{PROG} = Program time of last page + program time of the (last -1) page - (program command time + data loading time of last page).

9.7 Page Duplicate Program

The Page Duplicate program is configured to quickly and efficiently rewrite data stored in one full page to another page location without utilizing external memory. Since the time-consuming serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the block also needs to be copied to the newly assigned free block. A Page Duplicate program operation is performed by first initiating a read operation with command 35h and the address of the source which then duplicates the whole 2112 Byte data into the internal data buffer. As soon as the device is ready, the Program Confirm command (10h) is required to actually begin the programming operation to the address of the destination page. Once the Page Duplicate Program is finished, any additional partial page programming into the copied pages is prohibited before erasure.

The data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 9.11 on page 28.

Figure 9.11 Page Duplicate Program Operation

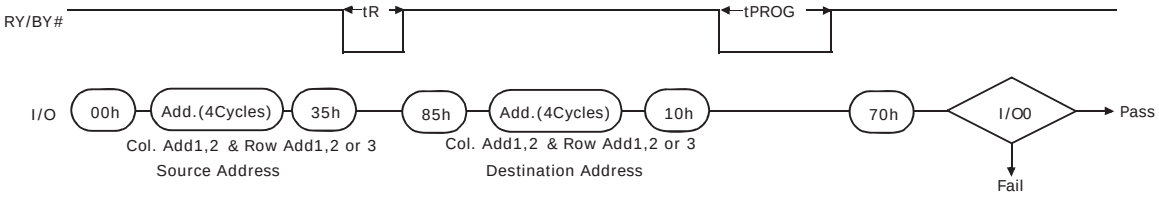
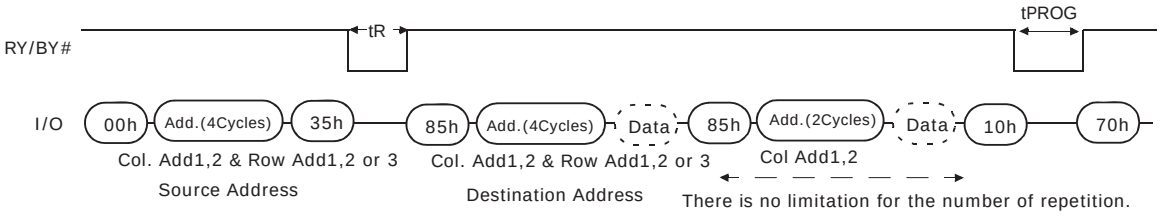


Figure 9.12 Page Duplicate Program Operation with Random Data Input



9.8 Block Erase and Erase Suspend

The Block Erase command sequence starts with the block erase setup command 60h, followed by two or three cycles of row address, followed by the block erase execute command D0h. Note that the page address part of the row address is ignored.

The Block Erase operation starts on the rising edge of WE# during the erase execute command. However, the Erase operation will not start if WP# is Low at this time or if the Erase command is addressing the OTP area after any OTP page has been protected.

Once t_{PRESUS} has elapsed, the Erase operation can be suspended by writing the Erase Suspend Command, FFh. RY/BY# or the status register may be monitored to determine when the erase is suspended, the device is ready, and it is safe to proceed with other commands. An Erase command with any address resumes the suspended Erase operation.

During Erase suspend any command operation on the erase block, except erase, is ignored. The following command operations in any other block are allowed:

- Full or partial page read
- Full or partial page program
- Read for page duplicate
- Page duplicate program
- Program Address or Data Change
- Read Column Address Change
- Read Status
- ID Read

Commands ignored during erase suspend:

- Pipeline Read
- Cache Program
- OTP Enter and Exit

The Reset or Erase Suspend command is prohibited during erase supend.

Figure 9.13 Block Erase

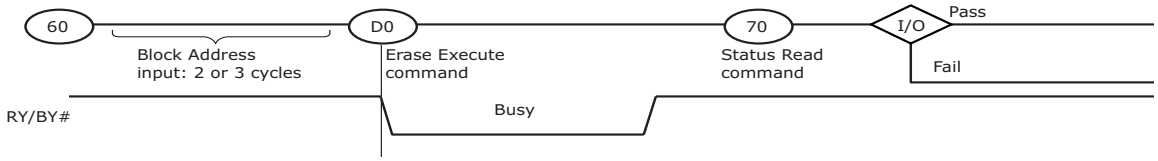
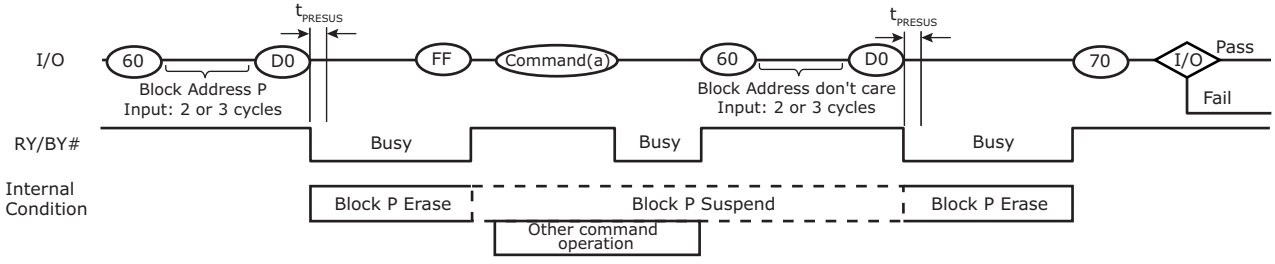


Figure 9.14 Erase Suspend Operation



9.9 Status

9.9.1 Status Read

The device contains a Status Register which may be read to find out whether a program or erase operation is completed, and whether the program or erase operation completed successfully. After writing a 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. The control by two lines allows the system to poll the progress of each device in multiple device connection even if the RY/BY# pins are common wired. RE# or CE# does not have to be toggled for update status. Refer to Table 9.7 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles. The Status Register clears after another valid command is entered, excluding a status read. An application example with multiple devices is shown in Figure 9.15.

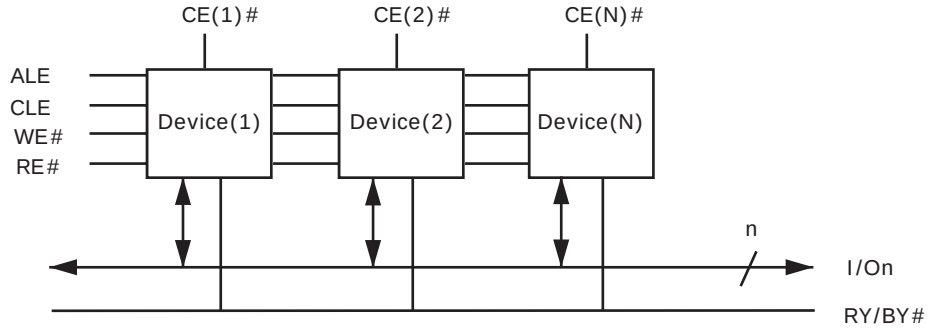
Table 9.7 Status Register Table

I/O	During Program/ Erase	Page Program	Block Erase	Cache Program	Read	Pipeline Read	Definition
I/O 0	Reserved	Pass/Fail	Pass/Fail	Pass/Fail(N)	Reserved	Reserved	0 = Pass; 1 = Fail
I/O 1	Reserved	Reserved	Completed/ Suspended (Note 3)	Pass/Fail(N-1)	Reserved	Reserved	0 = Pass, Completed; 1 = Fail, Suspend
I/O 2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
I/O 3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
I/O 4	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
I/O 5	Busy	True Ready/Busy	Ready/Busy	True Ready/Busy	Ready/Busy	True Ready/ Busy	0 = Busy; 1 = Ready
I/O 6	Busy	Cache Ready/Busy (Note 1)	Ready/Busy	Cache Ready/Busy (Note 1)	Ready/Busy	Cache Ready/ Busy (Note 4)	0 = Busy; 1 = Ready
I/O 7	Reserved	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	0 = Protected; 1 = Unprotected

Notes

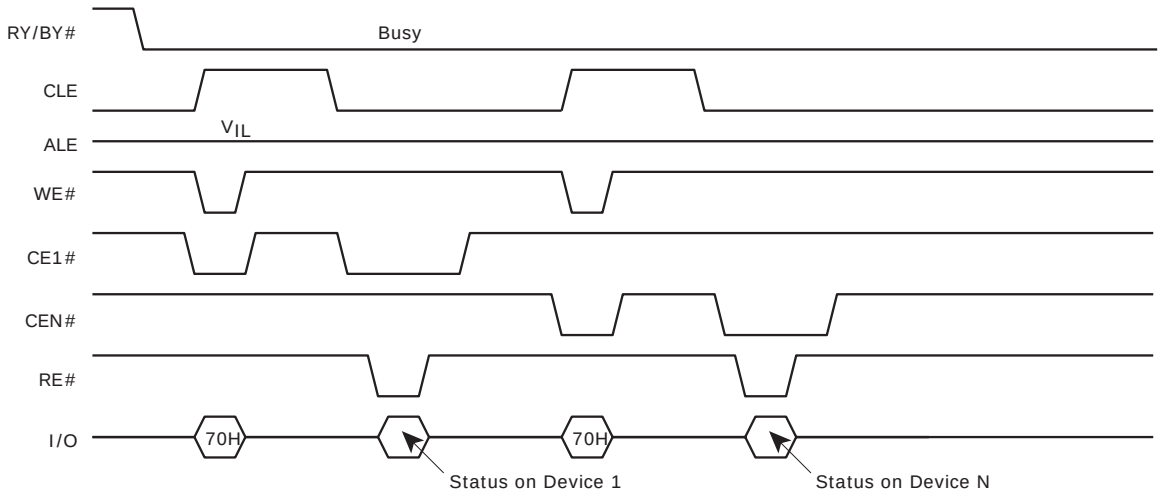
1. *True Ready/Busy represents internal program operation status which is being executed in cache program mode.*
2. *I/Os defined* as reserved *are recommended to be masked out when Read Status in being executed.*
3. *During an Erase suspended operation, I/O 1 will be able to hold the status which is in the Erase suspended condition, even if new a command is inputted.*
4. *True Ready/Busy represents internal the read operation status which is being executed in pipeline read mode.*

Figure 9.15 Multiple Devices



If the RY/BY# pin signals from multiple devices are wired together as shown in Figure 9.15, the Status Read function can be used to determine the status of each individual device.

Figure 9.16 Status Read Timing Application Example



9.9.2 Status After Power On or Reset

After Reset or Device power up the device goes through a power-on sequence as described in Section 9.2. After t_{PRE} has passed the status register will be in its cleared state. In the cleared state the status bits read 60h if WP# is Low or they will read E0h if WP# is high. This state indicates that internal operations are complete and the device is ready to accept commands

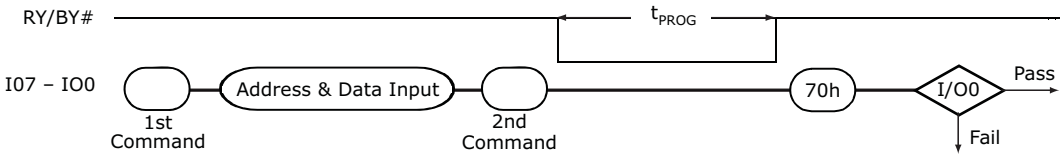
9.9.3 Status of Read, Program, or Erase

- Once a Read Program, or an Erase process starts, the Read Status Register command may be entered, followed by RE# and CE# Low, to read the status register.
- The system controller can detect the completion or failure of an operation by monitoring the RY/BY# output, or the Status bits (IO6 and IO5) of the Status Register.
  - RY/BY# is High during Ready and Low during Busy.
  - IO6 and IO5 are High during Ready and Low during Busy.
  - All other Status Bits are Reserved during Busy.
- Only the Read Status command and Reset command are valid while an operation is in progress.
- Successful completion, suspend, or failure of an operation results in a return to ready status.
- When the device is Ready (RY/BY#, IO6, and IO5 are High) the Write Status Bit (IO0) and Suspend Status Bit (IO1) may be checked
  - If Erase was the last operation before the device became ready, IO1 is Low if the Erase is completed and High if the Erase is suspended.
  - IO 0 is High if Program (or Erase) Error, or Low if Successful.
- The Status Register clears after another Execution command is entered.

  All 6 OTP commands will also clear the status registers because an embedded program occurs inside the device.

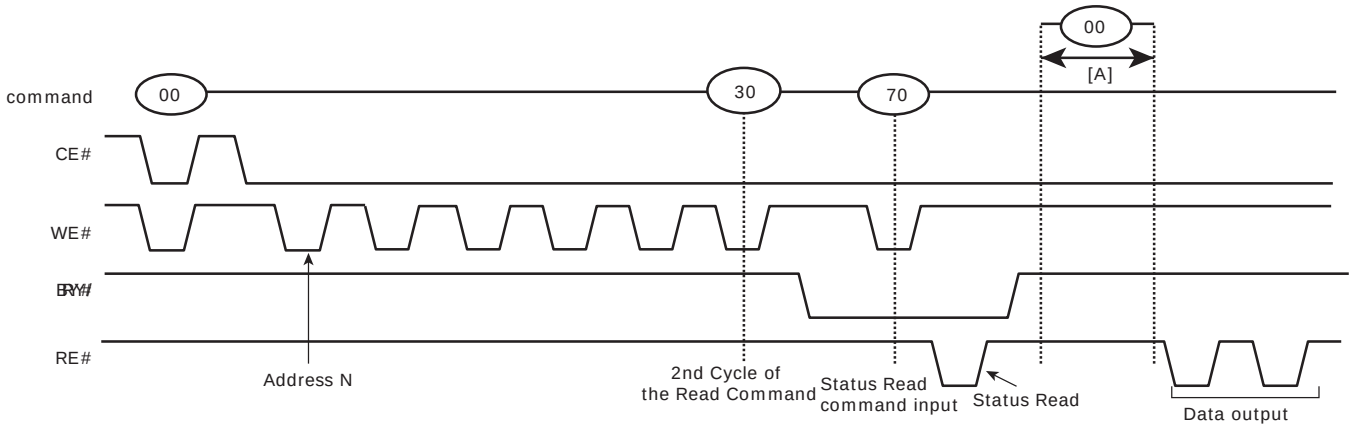
  Execution commands replace the status of the last operation with status of the operation initiated by the execution command. Execution commands are the commands that initiate a new operation. These are 30h, 31h, 32h, 33h, 35h, 10h, D0h, and FFh. However, the cache program execution command 15h clears only the N–1 (I/O 1) status and shifts the N (I/O 0) status to the N–1 status position. The Page register Ready/Busy (I/O 5) and Cache Register Ready / Busy (I/O 6) status bits remain valid.

Figure 9.17 RY/BY# During Program/Erase



9.9.4 Status Read During a Read Operation

Figure 9.18 Status Read During a Read Operation



The device status can be read by writing the Status Read command 70h in Read mode.

Once the device is set to Status Read mode by a 70h command, the device does not return to Read mode. However, when the Read command 00h is written during [A], the Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary.

When reading another page (example, address M), the following command patterns will be allowed;

(1) 00h --- Address N --- 30h --- 70h --- FFh --- 00h --- Address M --- 30h --- RE# toggle

(2) 00h --- Address N --- 30h --- 70h --- 00h --- 00h --- Address M --- 30h --- RE# toggle

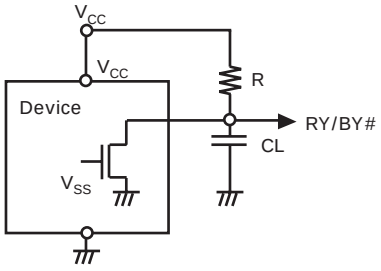
(3) 00h --- Address N --- 30h --- 70h --- 00h --- RE# toggle --- 00h --- Address M --- 30h --- RE# toggle

(4) 00h --- Address N --- 30h --- 70h --- 00h --- Address M --- 30h --- RE# toggle

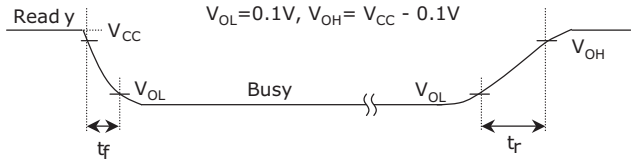
In these cases, from the last 30h, the page data of Address M is read out by the RE# toggle.

A pull-up resistor must be used for termination because the RY/BY# buffer consists of an open drain circuit.

Figure 9.19 RY/BY#: Termination for the Ready/Busy Pin (RY/BY#)



This data may vary from device to device.
Use this data as a reference when selecting a resistor value.



$$R = \frac{V_{CC}\ max - V_{OL}}{I_{OL} + I_L} = \frac{1.85\ V}{3\ mA + I_L}$$

9.10 OTP

The device includes a One Time Protection (OTP) area of memory separate from the normal memory array that may be permanently locked to secure data. The OTP area contains 8 pages, each of which can be individually locked to prevent program or erase. The commands for the OTP area are shown in Table 9.1.

The system accesses the OTP pages by overlaying them into block 0 of the Main Array. The OTP default commands determine the OTP overlay status at power-on for the life of the device. Once one of the OTP default overlay commands is entered, the default cannot be changed. It is recommended that the OTP default be set during factory programming to prevent the default overlay from being changed after the device leaves the factory.

If the system does not want the OTP overlayed at power-on, the “OTP Default as Removed” command should be issued during factory programming. To set the device so that the OTP area is overlayed at power-on, the system must issue the “OTP Area Default as Overlay” during factory programming. This is the configuration that should be used for systems that utilize the power-on read feature for boot. In this configuration, Pages 8 through 63 of block 0 will not be accessible.

Once the default is set, the OTP overlay can be adjusted using the “OTP Area Overlay” and “OTP Area Remove Commands”. These commands allow the system to determine whether the addresses for block 0 will map to the OTP pages or main array pages.

The “OTP Page Protect” command is used to individually lock the pages and prevent further programming. After one of the OTP pages is protected, none of the remaining OTP pages are able to erase, since they are all part of the same block. The remaining unlocked pages can be programmed and they must be individually locked to secure the data from being overwritten. It is recommended that the pages be protected after they are programmed.

Figure 9.20 OTP Commands

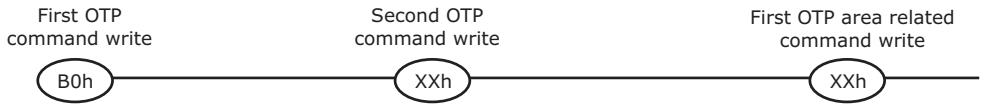


Figure 9.21 OTP Page Protect Command Sequence Diagram

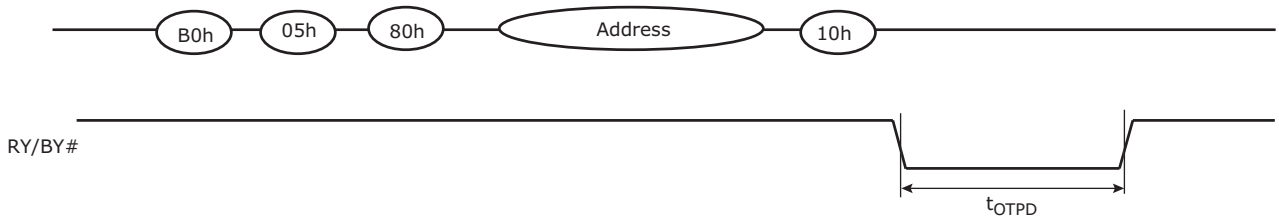
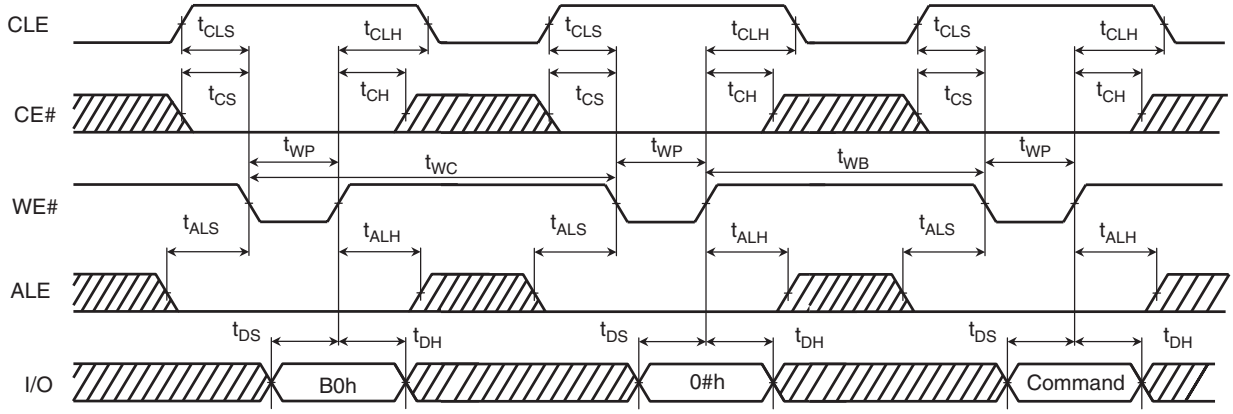
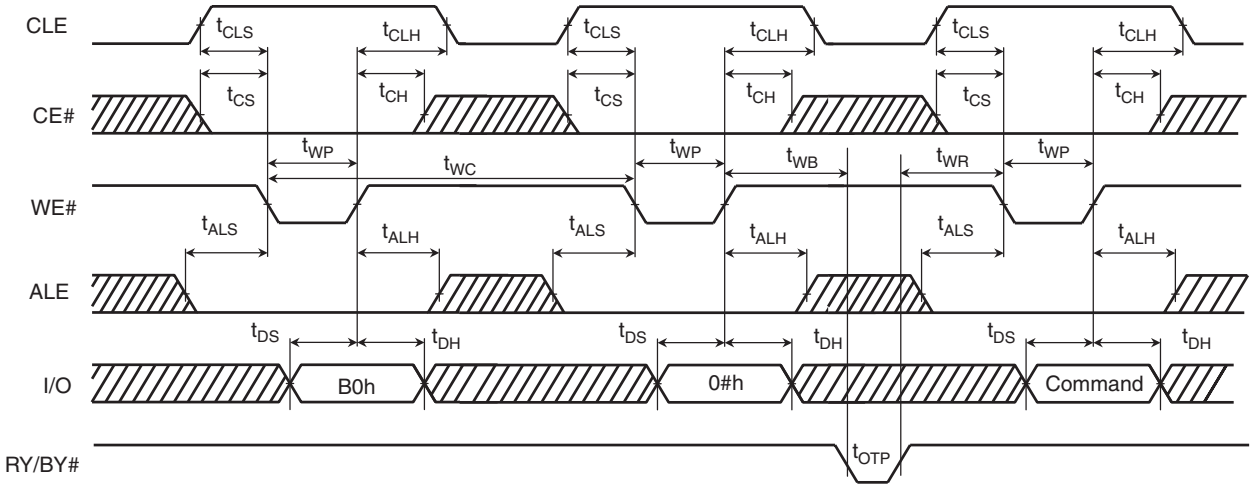


Figure 9.22 OTP Command (Page Protection Status) Timing Diagram



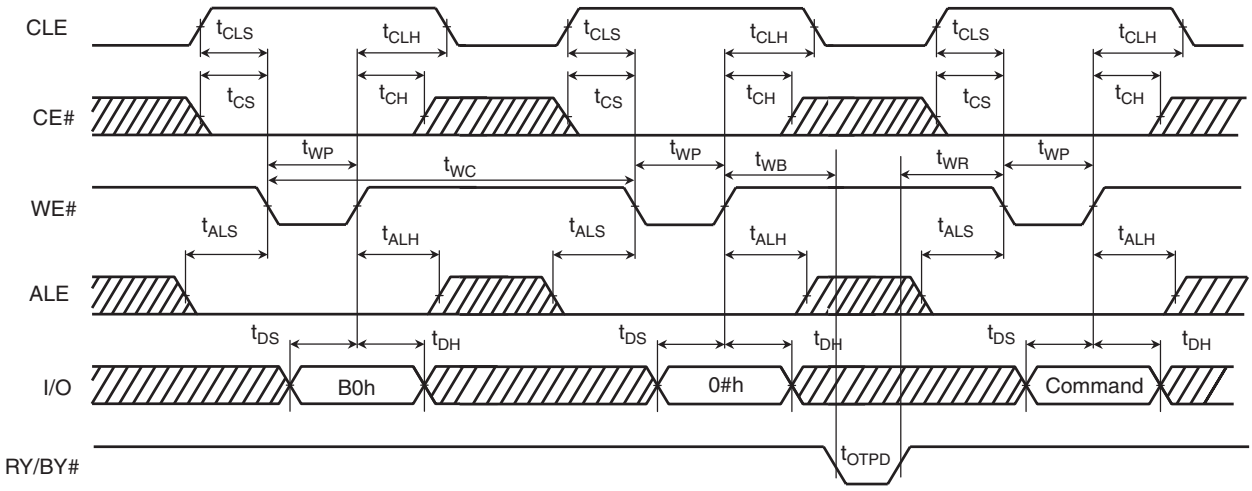
Note
0#h is 2nd cycle command for OTP. # is 2.

Figure 9.23 OTP Command (Overlay/Remove) Timing Diagram



Note
0#h is 2nd cycle command for OTP. # is 0 or 1.

Figure 9.24 OTP Command (Default as Overlay/Default as Removed) Timing Diagram



Note
0#h is 2nd cycle command for OTP. # is 3 or 4.

9.11 Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 V and the device enters standby.

The response to an *FFh* Reset command input during the various device operations is shown in Figure 9.25 to Figure 9.29.

Figure 9.25 Reset (FFh) Command Input During Programming

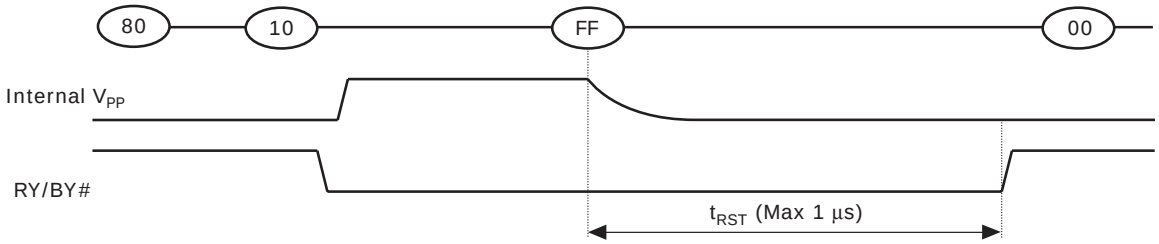


Figure 9.26 Reset (FFh) Command Input During Erasing

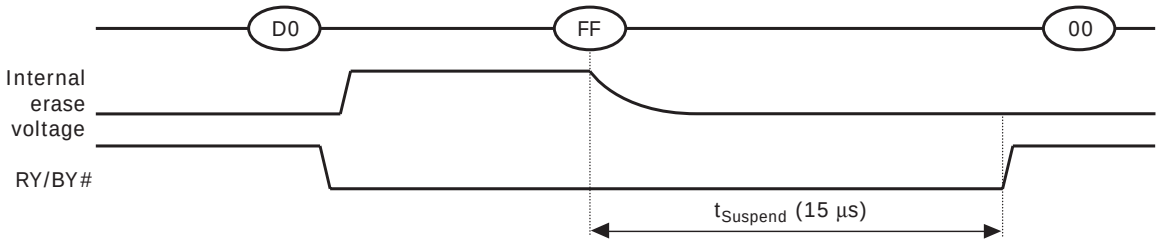


Figure 9.27 Reset (FFh) Command Input During a Read Operation

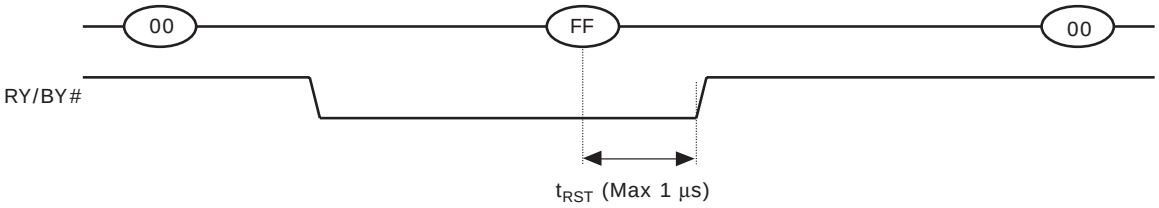


Figure 9.28 Status Read Command (70h) Input After a Reset

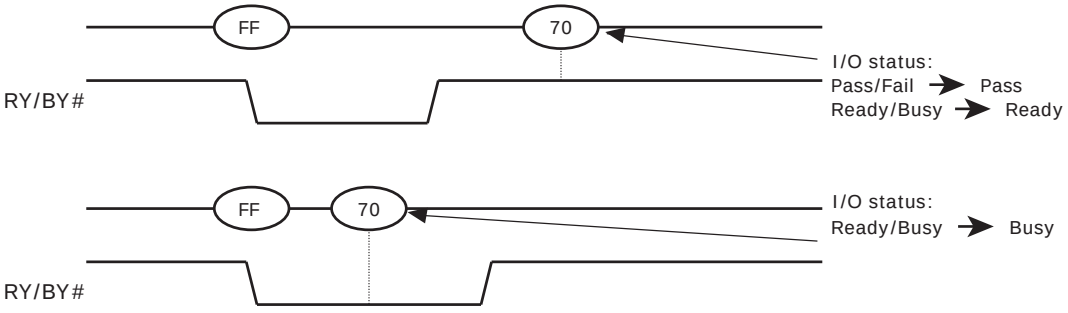
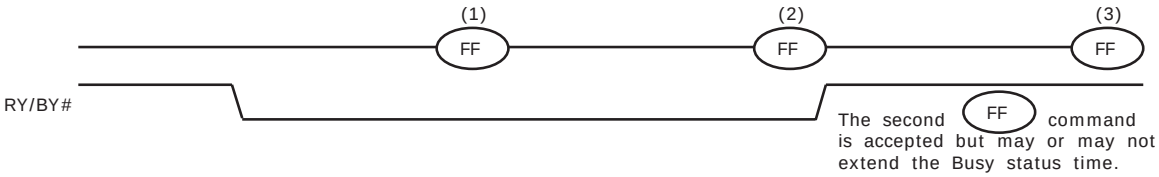


Figure 9.29 Two or More Reset Commands Input in Succession



10. Electrical Specifications

10.1 Absolute Maximum Ratings

Table 10.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN/OUT}$	–0.5 to V_{CC} + 0.5	V
	V_{CC}	–0.5 to + 2.5	
Storage Temperature	T_{STG}	–65 to +150	°C
Operating Temperature	T_{OPR}	–25 to +85 (Wireless)	°C
Temperature under bias	T_{BIAS}	–65 to +125	°C
Short circuit current	I_{OS}	5	mA

1. *Notes*
2. *Minimum DC voltage is –0.6 V on input/output pins. During transitions, this level may undershoot to –2.0 V for periods < 30 ns.*
3. *Maximum DC voltage on input/output pins is V_{CC} +0.3 V which, during transitions, may overshoot to V_{CC}+2.0 V for periods < 20 ns.*
4. *Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

10.2 Recommended DC Operating Conditions

Table 10.2 Recommended DC Operating Conditions

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	1.7	1.8	1.95	V
V_{SS}	Power Supply Voltage	0	0	0	V

10.3 DC Characteristics

Table 10.3 DC Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	V_{CC} active read current (average during read cycle)	t_{RC} = 25 ns, I_{OUT} = 0 mA	—	40	50	mA
I_{CC2}	Program current	—	—	60	75	mA
I_{CC3}	Erase Current (standard mode)	—	—	60	75	mA
I_{SB1}	Stand-by Current (TTL)	CE# = V_{IH}, WP# = V_{IL}	—	—	1	mA
I_{SB2}	Stand-by Current (CMOS)	CE# = V_{CC} –0.2 V, WP# = 0.2 V All other pins = –0.1 V	—	10	60	µA
I_{LI}	Input Leakage Current	V_{IN} = 0 to V_{CC}, V_{CC}= V_{CC} max	—	—	±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to V_{CC}, V_{CC}= V_{CC} max	—	—	±1	µA
V_{IH} (note 1)	Input High Voltage		V_{CC} - 0.4	—	V_{CC} + 0.2	V
V_{IL} (note 2)	Input Low Voltage	—	–0.3	—	0.4	V
V_{OH}	Output High Voltage Level	I_{OH} = –100 µA, V_{CC}= V_{CC}min	V_{CC} - 0.1	—	—	V
V_{OL}	Output Low Voltage Level	I_{OL} = 100 µA, V_{CC}= V_{CC} min	—	—	0.1	V
I_{OL}	Output Low Current (RY/BY#)	V_{OL} = 0.1 V	1	1.4	—	mA

Notes

1. *V_{IH} can overshoot to V_{CC} +0.4 V for durations of 20 ns or less.*
2. *V_{IL} can undershoot to –0.4 V for durations of 20 ns or less.*
3. *CE# is 15 pF, WP# = 18 pF, CLE = 18 pF*

10.4 Capacitance

Table 10.4 Capacitance (T_a = 25°C, f = 1 MHz)

Parameter Symbol	Parameter Description	Test Condition	Density	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	512 Mb	—	10	pF
			1 Gb	—	10	pF
			2 Gb	—	10	pF
			4 Gb	—	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	512 Mb	—	10	pF
			1 Gb	—	10	pF
			2 Gb	—	10	pF
			4 Gb	—	20	pF

Notes

1. *Test conditions T_a = 25°C, f = 1.0 MHz*
2. *Sampled, not 100% tested.*
3. *CE is 15 pf.*
4. *WP is 18 pf.*
5. *CLE is 18 pf.*

10.5 AC Test Conditions

Table 10.5 AC Test Conditions

Operating Range	V_{CC} 1.7 V to 1.95 V
Input level	0.0 to V_{CC}
Input comparison level	$V_{CC}/2$
Output data comparison level	$V_{CC}/2$
Load capacitance (C_L)	30 pF
Transition time (t_T) (input rise and fall times)	5 ns

10.6 Valid Blocks

Table 10.6 Valid Blocks

Parameter Symbol	Parameter Description	Density	Min.	Typ.	Max.	Unit
N_{VB}	Number of Valid Blocks	512 Mb	512	—	512	Blocks
		1 Gb	1024	—	1024	Blocks
		2 Gb	2048	—	2048	Blocks
		4 Gb	4096	—	4096	Blocks

10.7 AC Characteristics

Table 10.7 AC Characteristics (Sheet 1 of 2)

Parameter Symbols	Description	Min.	Max.	Unit
t_{CLS}	CLE Setup Time	0	—	ns
t_{CLH}	CLE Hold Time	8	—	ns
t_{CS}	CE# Setup Time	0	—	ns
t_{CH}	CE# Hold Time	8	—	ns
t_{WP}	Write Pulse Width	15	—	ns
t_{ALS}	ALE Setup Time	0	—	ns
t_{ALH}	ALE Hold Time	8	—	ns
t_{DS}	Data Setup Time	15	—	ns
t_{DH}	Data Hold Time	8	—	ns
t_{WC}	Write Cycle Time	25	—	ns
t_{WH}	WE# High Hold Time	10	—	ns
t_{WW}	WP# High to WE# Low	100	—	ns
t_{RR}	Ready to RE# Falling Edge	20	—	ns
t_{RW}	Ready to WE# Falling Edge	20	—	ns
t_{RP}	Read Pulse Width	17	—	ns
t_{RC}	Read Cycle Time	25	—	ns
t_{REA}	RE# Access Time	—	17	ns
t_{CR}	CE# to RE# Time	0		ns
t_{AR}	ALE to RE# Time	10		ns
t_{CLR}	CLE to RE# Time	0		ns
t_{OH}	Data Output Hold Time	5	—	ns
t_{RHZ}	RE# High to Output High Impedance	—	15	ns
t_{CHZ}	CE# High to Output High Impedance	—	15	ns
t_{REH}	RE# High Hold Time	8	—	ns
t_{IR}	Output High Impedance to RE# Falling Edge	0	—	ns

Table 10.7 AC Characteristics (Sheet 2 of 2)

Parameter Symbols	Description	Min.	Max.	Unit
t_{RHW}	RE# High to WE# Low	30	—	ns
t_{WHC}	WE# High to CE# Low	30	—	ns
t_{WHR}	WE# High to RE# Low	60	—	ns
t_R	Full Page Data Transfer from Memory Cell Array to Register	—	28	µs
	Partial Page Data Transfer from Memory Cell Array to Register	—	10	
t_{PT}	Pipeline Transfer	0.4	28	µs
t_{WB}	WE# High to Busy	—	100	ns
t_{RST}	Device Resetting Time (Read/Program)	—	6	µs
t_{PRE}	Power on Reset and Full Page Read	—	250	µs
$t_{SUSPEND}$	WE# High during Reset command to RY/BY# High	—	30	µs
t_{PRESUS}	Preamble time for suspended operation	—	10	µs
t_{OTP}	OTP Busy Time	—	5	µs
t_{OTPD}	OTP Default Busy Time	—	200	µs

10.8 Timing Diagrams

Figure 10.1 Command Input Cycle Timing Diagram

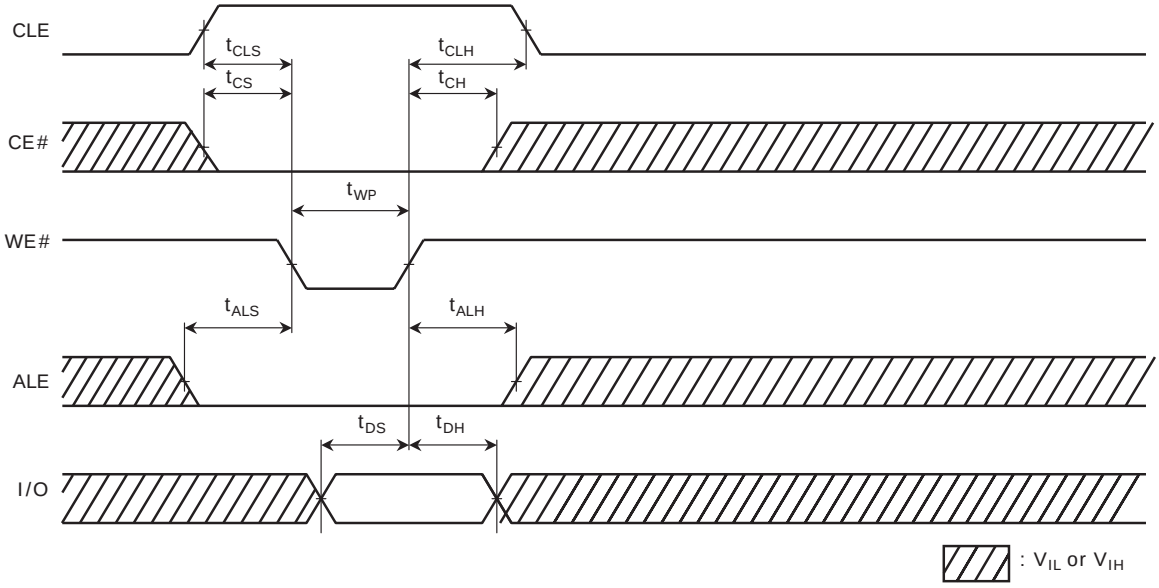


Figure 10.2 Address Input Cycle Timing Diagram (512 Mbit/1 Gbit)

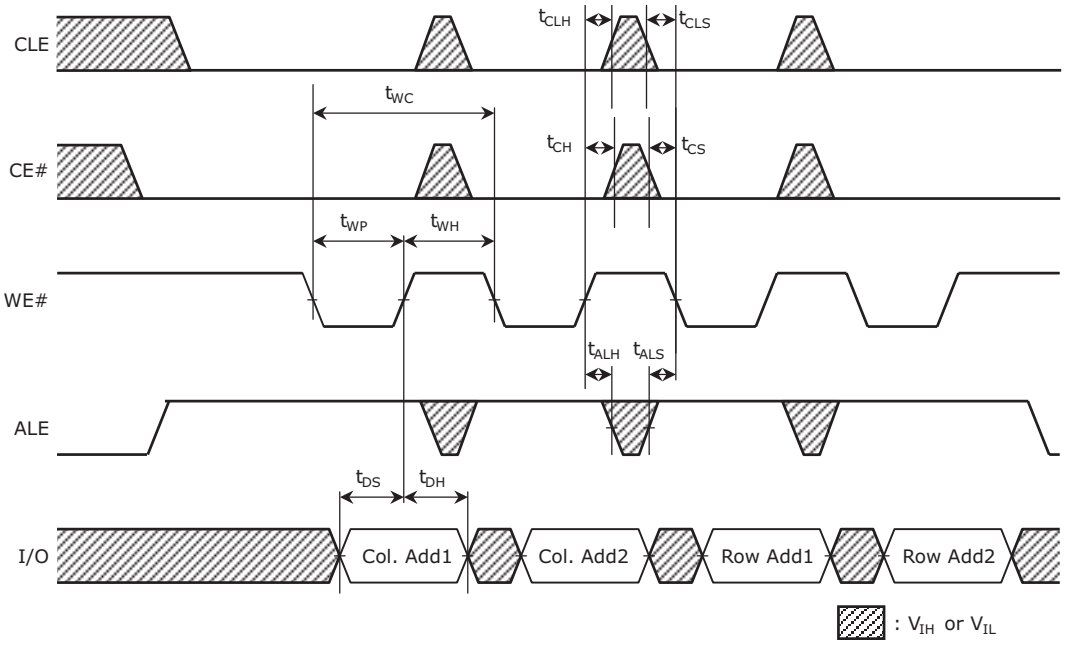


Figure 10.3 Address Input Cycle Timing Diagram (2 Gbit/4 Gbit)

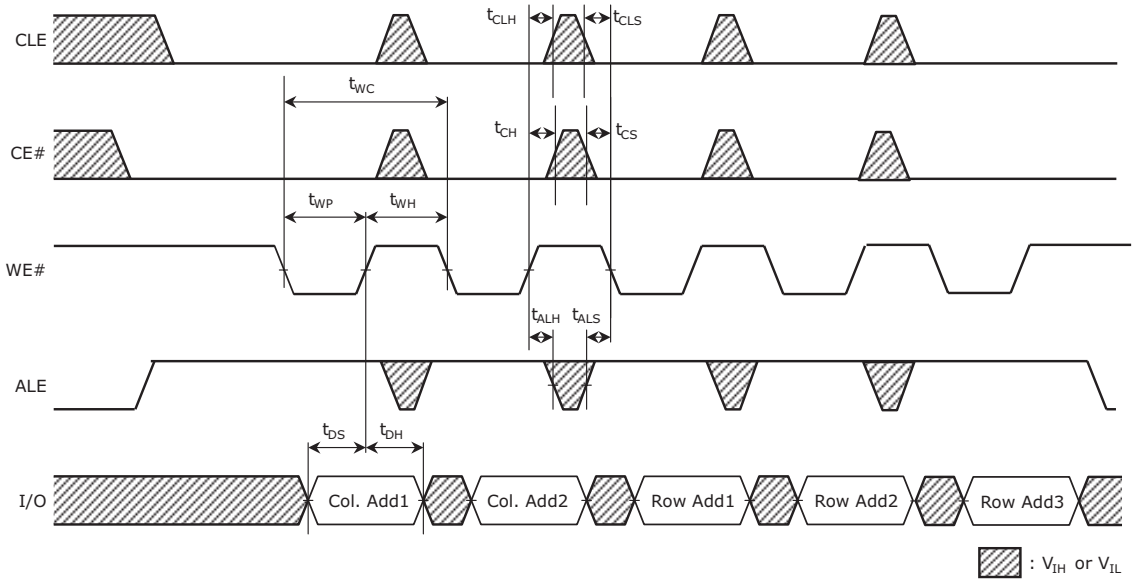


Figure 10.4 Data Input Cycle Timing Diagram

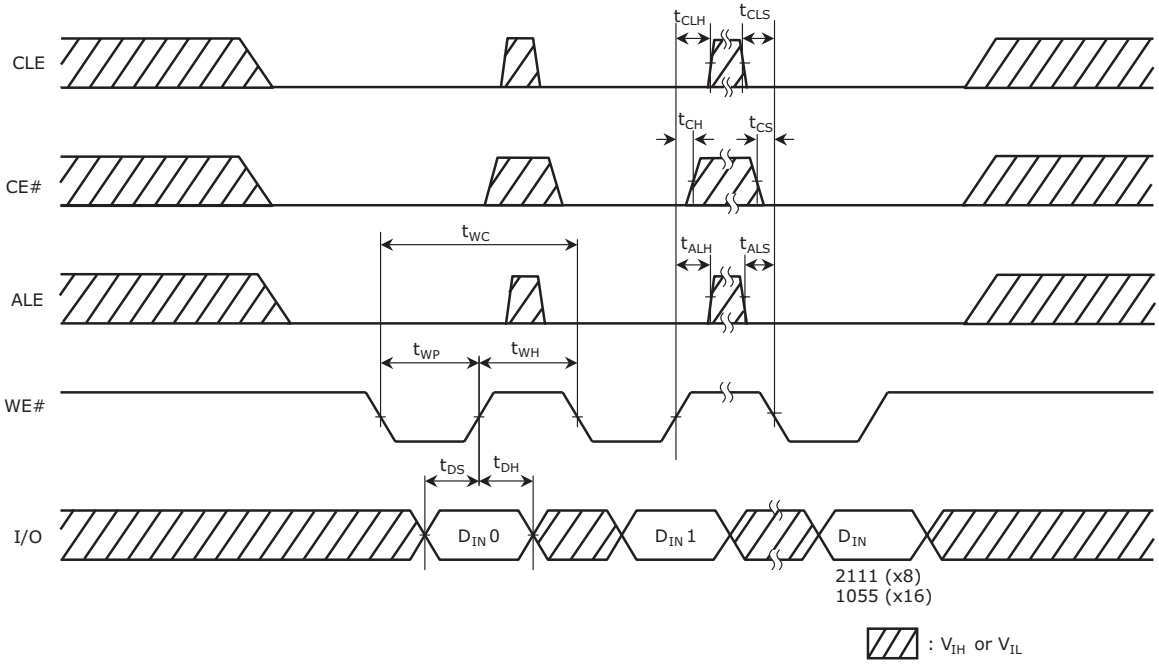


Figure 10.5 Serial Read Cycle Timing Diagram

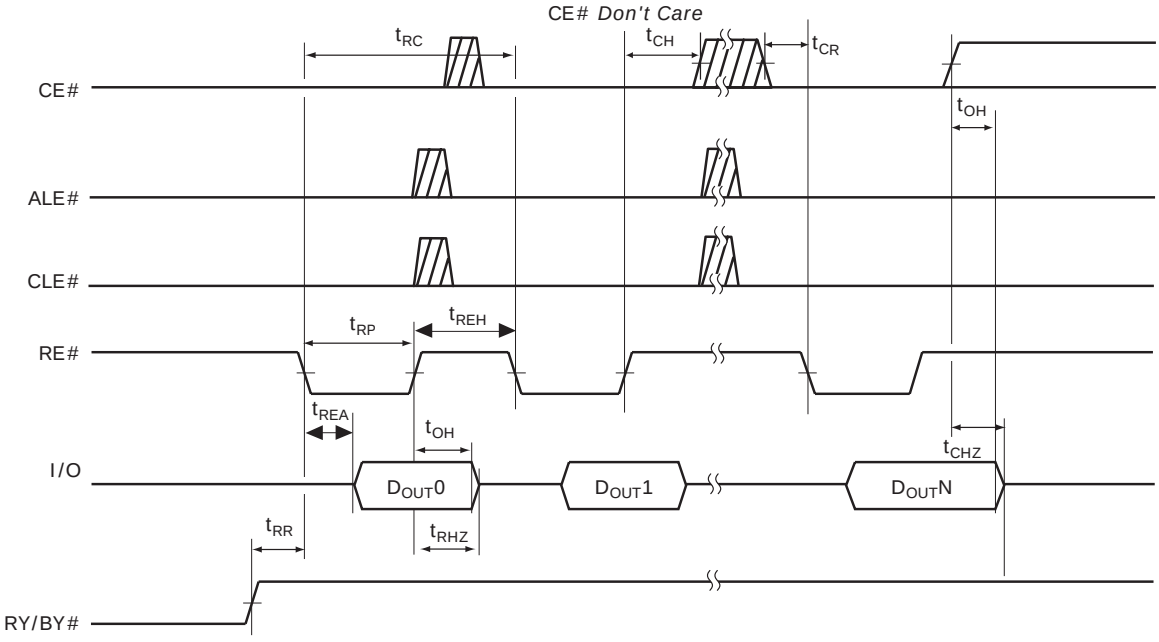


Figure 10.6 Status Read Cycle Timing Diagram

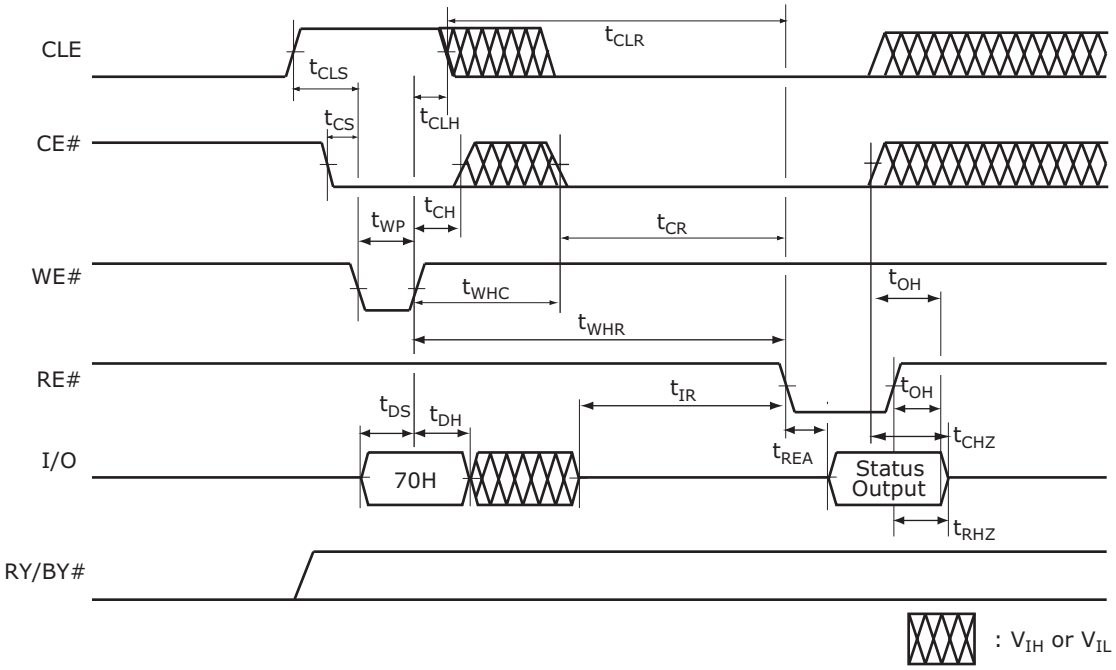
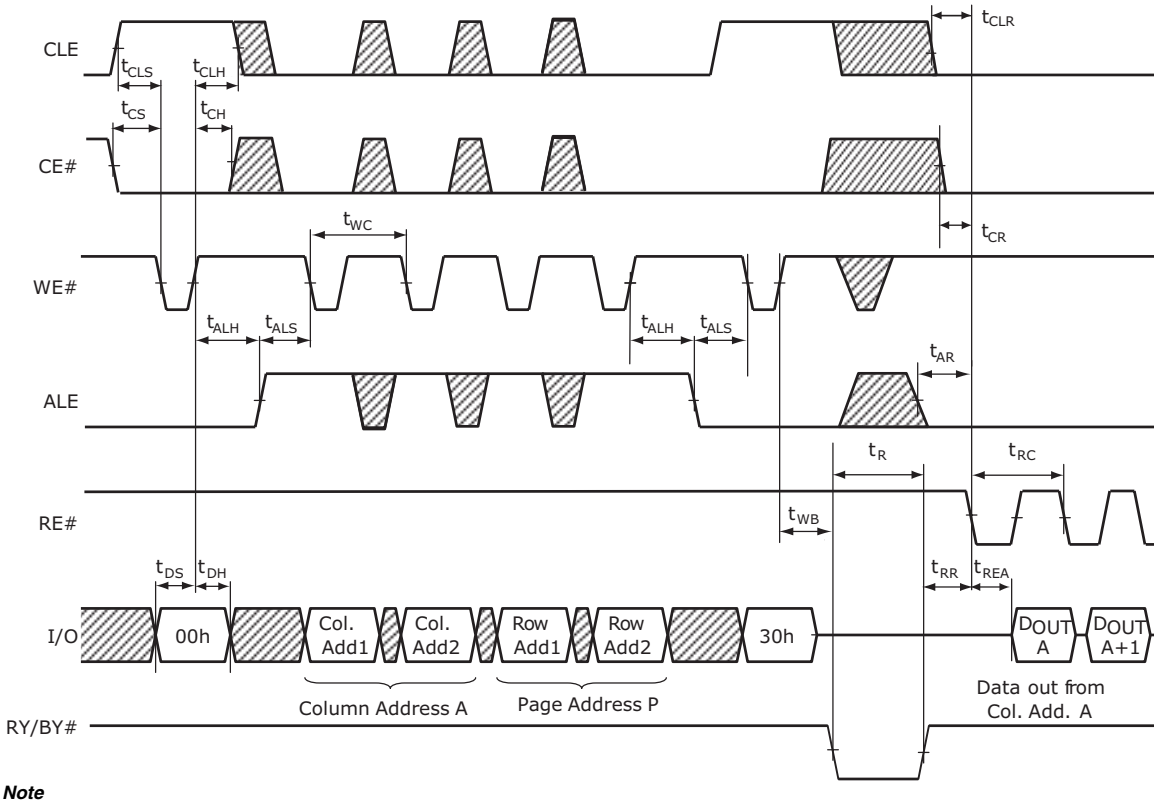
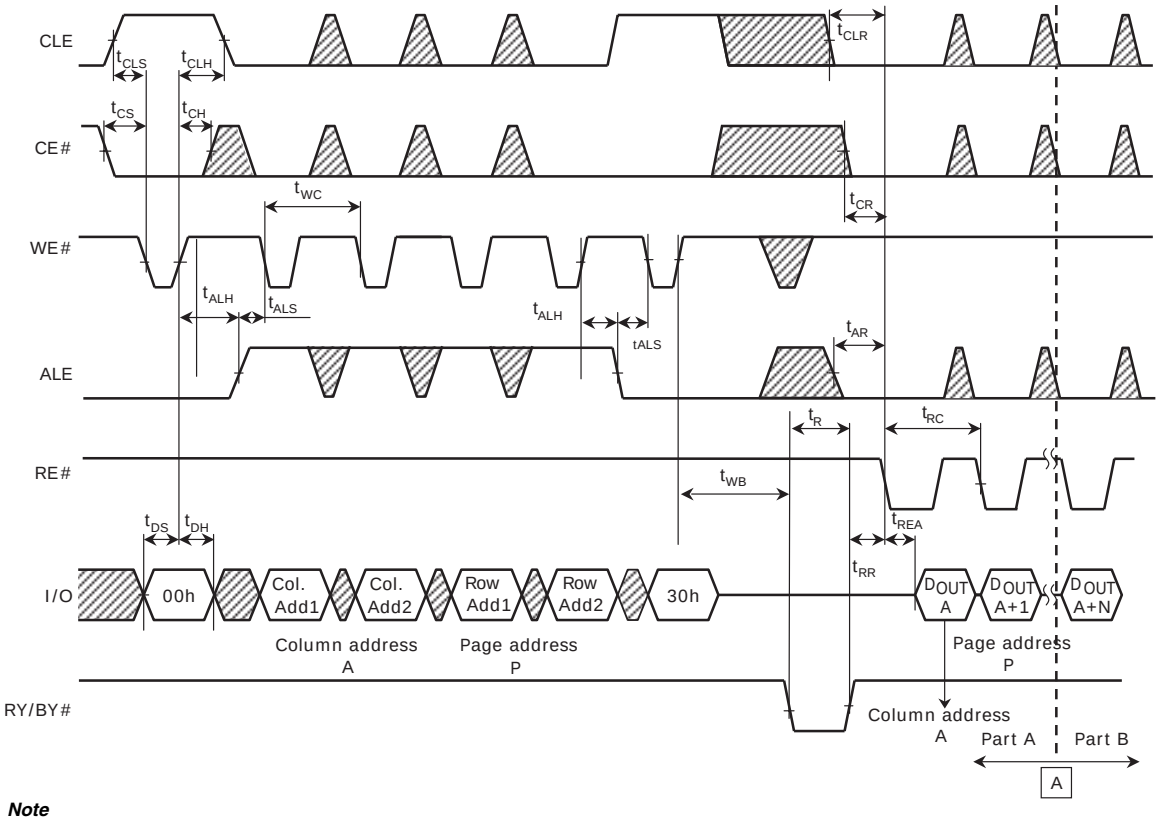


Figure 10.7 Read Cycle Timing Diagram



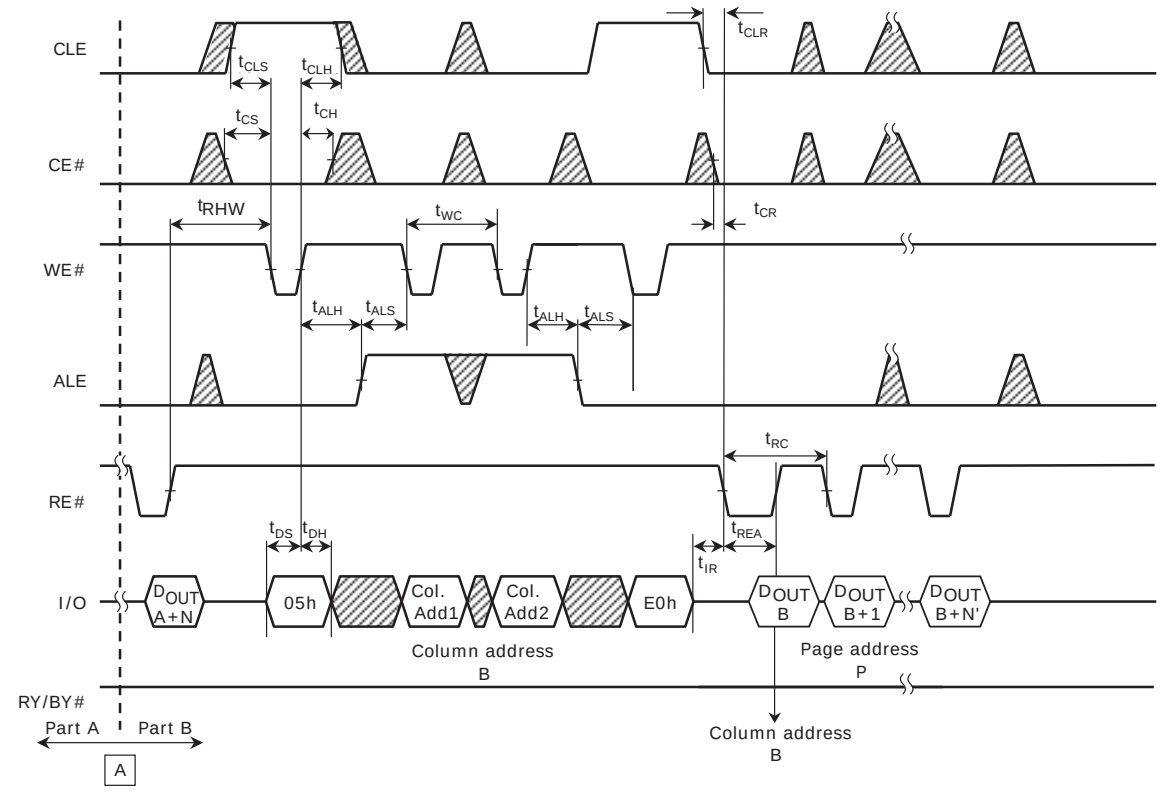
Note
In 2 Gbit/4 Gbit, Page Address is needed to input 3-cycles.

Figure 10.8 Column Address Change in Read Cycle Timing Diagram (1/2)



Note
In 2 Gbit/4 Gbit, Page Address is needed to input 3-cycles.

Figure 10.9 Column Address Change in Read Cycle Timing Diagram (2/2)



10.8.1 Program and Erase Characteristics

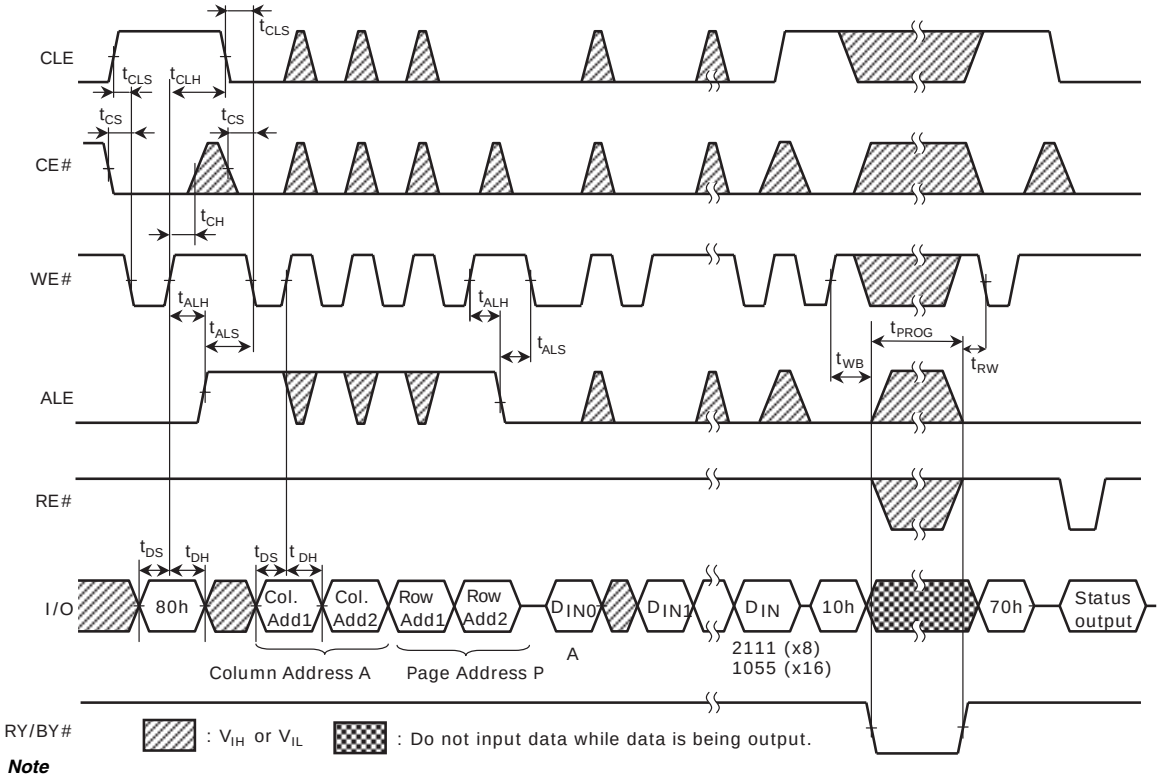
Table 10.8 Program and Erase Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CBSY1}	Dummy Busy Time for Cache Programming (Note 2)	—	0.4	0.8	µs
t_{CBSY2}	Dummy Busy Time for Cache Programming (Note 3)	—	(Note 4)	(Note 4)	µs
t_{PROG}	Page Programming Time	—	800	5000	µs
t_{PPROG}	Segment Programming Time	—	260	1400	µs
N	Number of Programming Cycles on Same Page (Note 1)	—	—	8	
t_{BERASE}	Block Erasing Time	—	50	150	ms
P/E	Number of Program/Erase Cycles (Notes 5, 6)	10,000	100,000	—	cycles

Notes

1. *One programming cycle per segment. Refer to Page Program on page 24 for more information.*
2. *First cache programming of a sequence.*
3. *Following cache programming of a sequence - second page and following pages.*
4. *Calculation method for t_{CBSY2} is the following:*
   - $t_{CBSY2} = t_{PROG}$ - (Command Cycles + t_{WC} x Number of Data Input Cycles)
5. *Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 10,000 cycles; checkerboard data pattern.*
6. *Under worst case conditions of 90°C, V_{CC}=1.70 V, 100,000 cycles.*

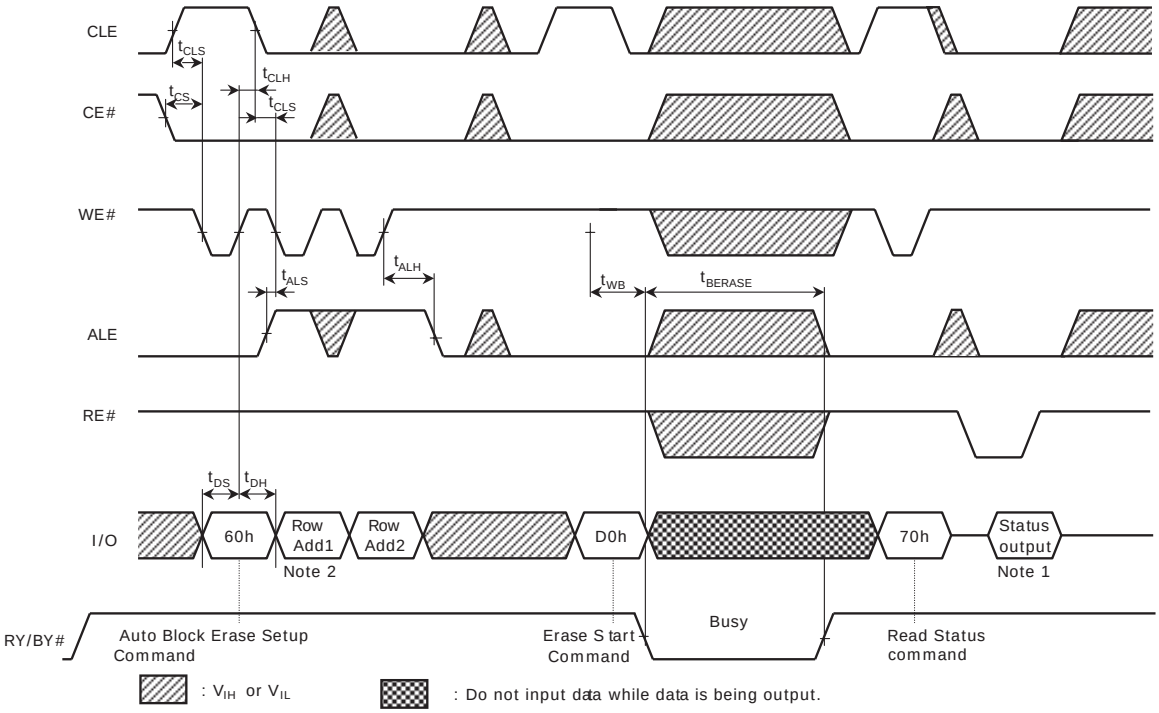
Figure 10.10 Program Operation Timing Diagram



Note

In 2 Gbit/4 Gbit, Page Address is needed to input 3-cycles.

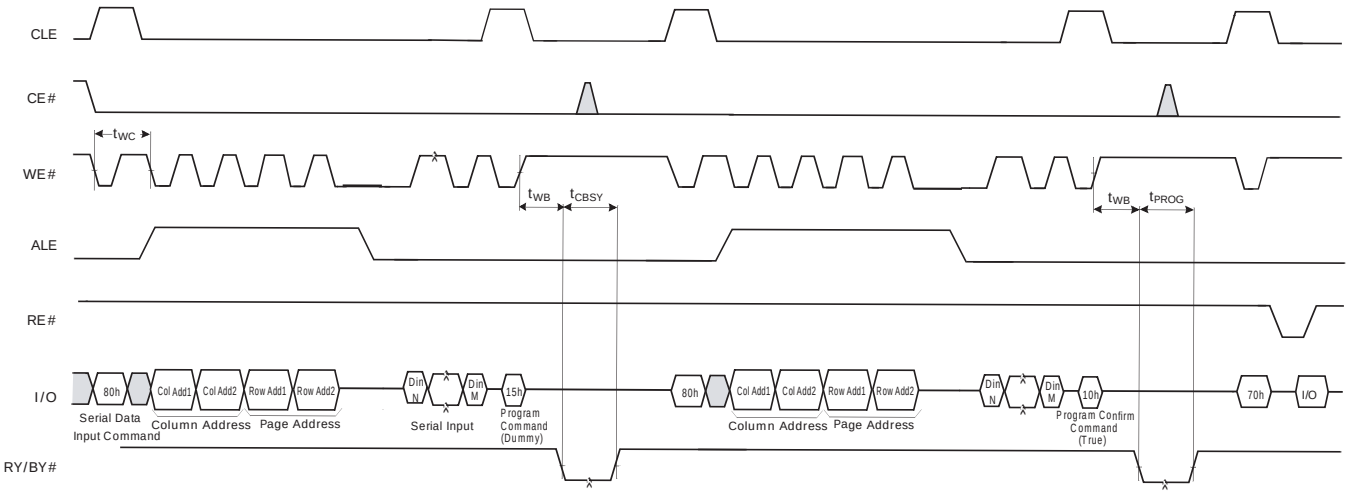
Figure 10.11 Block Erase Timing Diagram



Notes

1. *If I/O 0 =* 0*, then the erase is successful. If I/O 0 =* 1*, then there is an error in the erase.*
2. *Only the block address part of the* Row Address *bytes are used; page address is ignored.*
3. *In 2 Gbit/4 Gbit, Page Address is needed to input 3-cycles.*

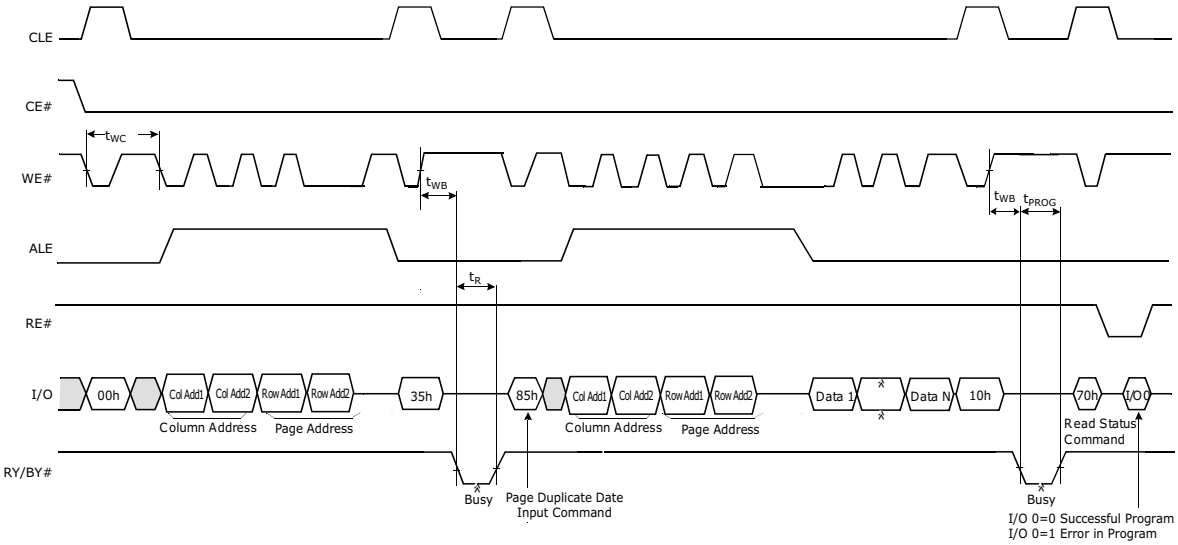
Figure 10.12 Cache Program Operation Timing Diagram



Note

1. *CE#, CLE, and ALE are Don't care.*
2. *In 2 Gbit/4 Gbit, Page Address is needed to input 3-cycles.*

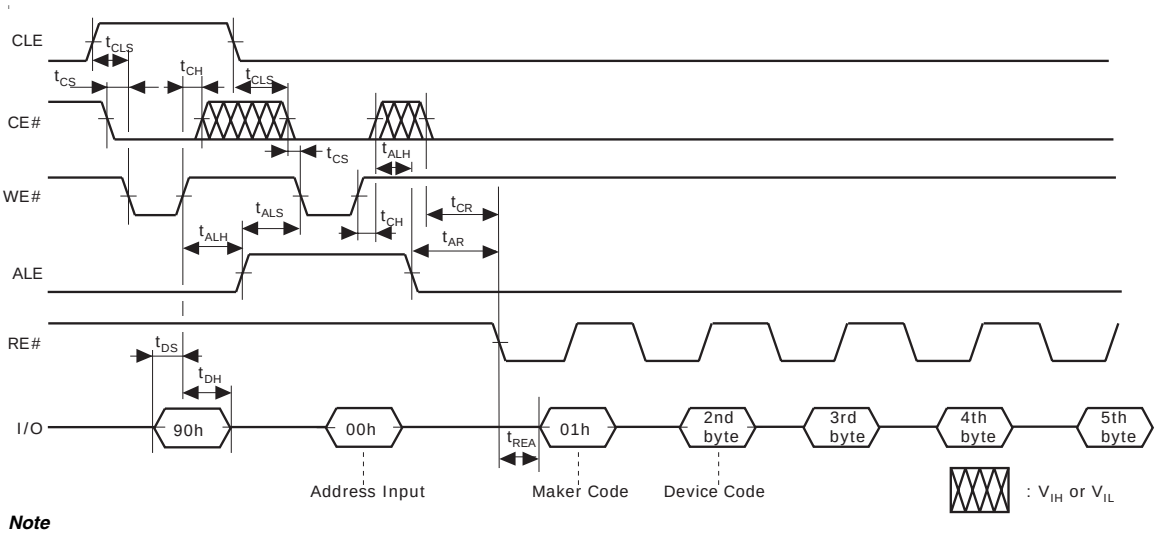
Figure 10.13 Page Duplicate Program Operation with Random Data Input Timing Diagram



Notes

1. *CE#, CLE, and ALE are Don't care.*
2. *In 2 Gbit/4 Gbit, Page Address is needed to input 3-cycles.*

Figure 10.14 ID Read Operation Timing Diagram



Note

CE#, CLE, and ALE are Don't care.

11. Revision History

Section	Description
Revision 01 (January 17, 2007)	
	Initial Release
Revision 02 (March 22, 2007)	
Block Erase	Clarified command restrictions
DC Characteristics	Changed I_{CC1}, I_{CC2}, and I_{CC3} values and definitions
Page Program	Clarified command restrictions
AC Characteristics	Changed t_{PRESUS} value Changed t_R value Changed t_{PRE} value Capacitance: Changed CE#, WP# and CLE capacitance values Clarified Erase Suspend Operation Status Bit: Clarified I/O 0 behavior during Erase Suspend
Revision 03 (September 27, 2007)	
Global	Deleted reference to 4 Gb ORNAND device
DC Characteristics	Changed Typical and Max specifications for I_{CC2} and I_{CC3}
Revision 04 (November 2, 2007)	
AC Characteristics	Changed t_{OTPD} value Changed $t_{SUSPEND}$ value Changed t_{CHZ} value Changed t_{RHZ} value Changed t_{RST} value Changed t_R Partial Page Data Transfer from Memory Cell Array to Register value Changed t_{CR} value Changed t_{CLR} value
DC Characteristics	Changed I_{OL} value
Program and Erase Characteristics	Changed t_{PROG} and t_{PPROG} value
Global	Defined 3 quality grades

Colophon

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